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MS-7778 VER: 0A

uATX 9.6" x 9.6"

CPU:

AMD FM2

System Chipset:

AMD - Hudson D3

On Board Chipset:

Fintek Super I/O -- F71808A

LAN -- Atheros AR8161L

HD Codec -- IDT 92HD73E

BIOS -- SPI ROM 64M

Main Memory:

DDR III X 4 (Max 16GB)

Expansion Slots:

PCI Express X16 Slot * 1

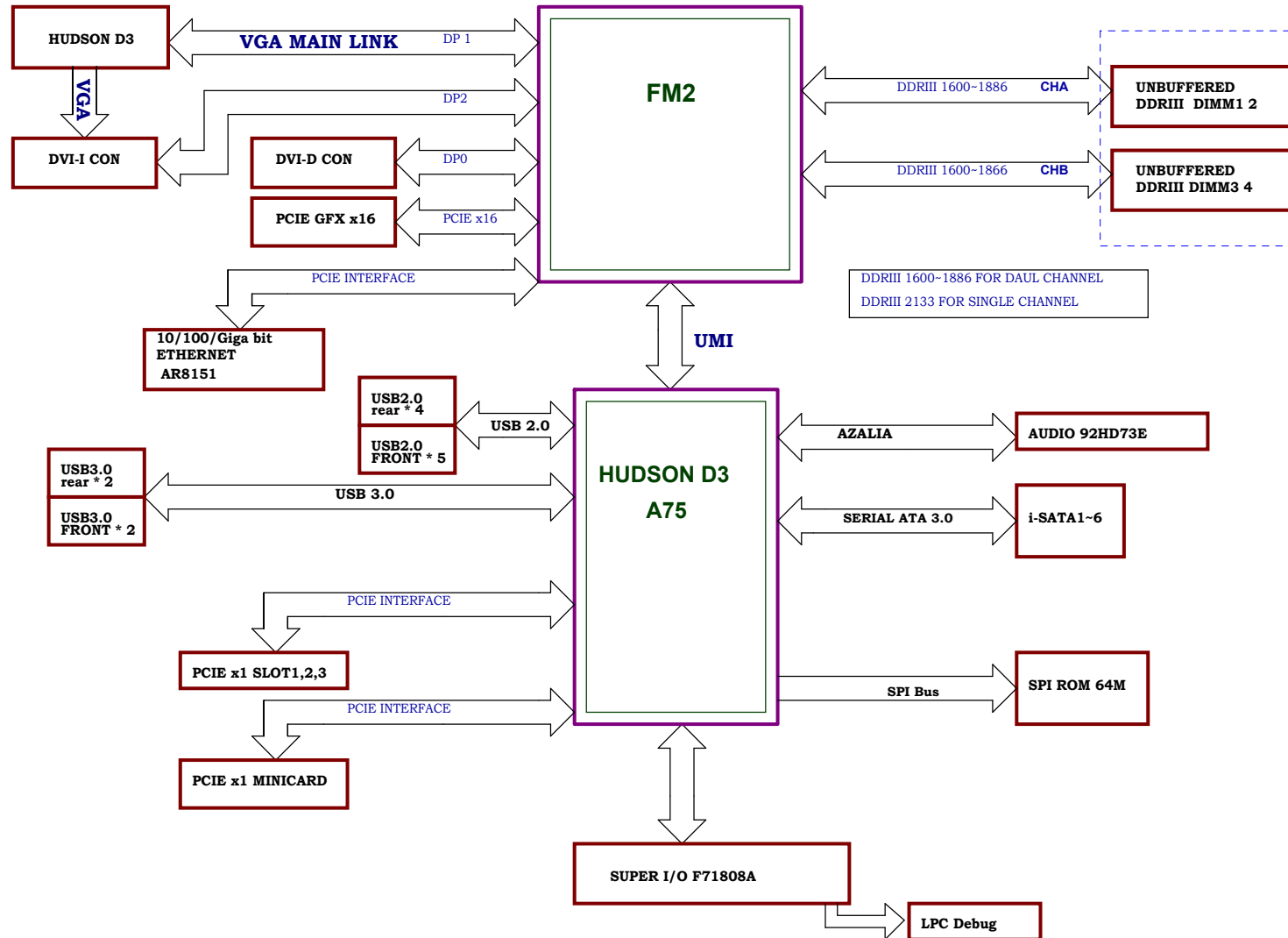
PCI Express X1 Slot * 3

PCI Express X1 Slot *1 for MINI CARD

PWM:

Controller -- Intersil ISL6277

FUSION BLOCK DIAGRAM



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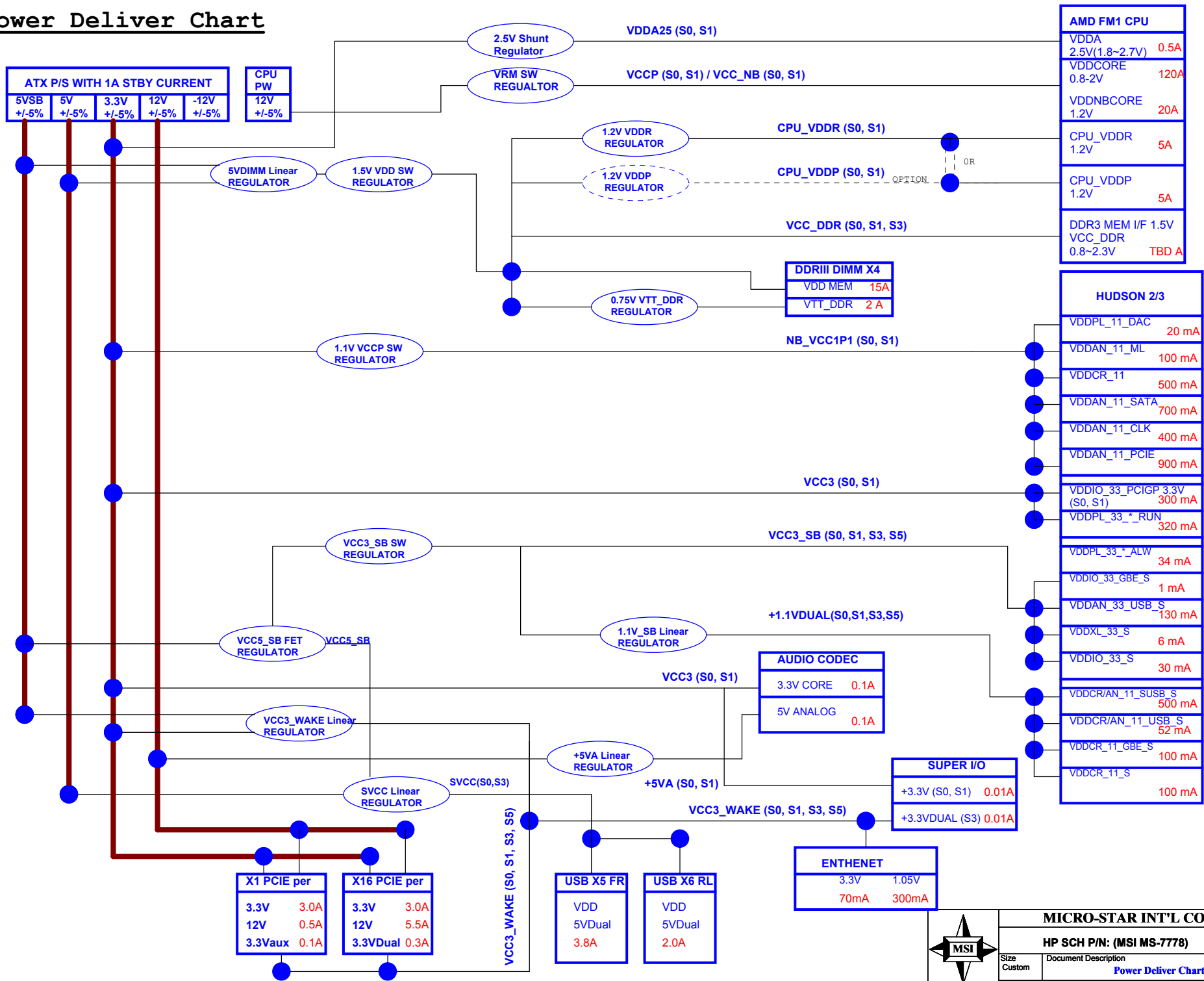
BLOCK DIAGRAM

Rev
0A

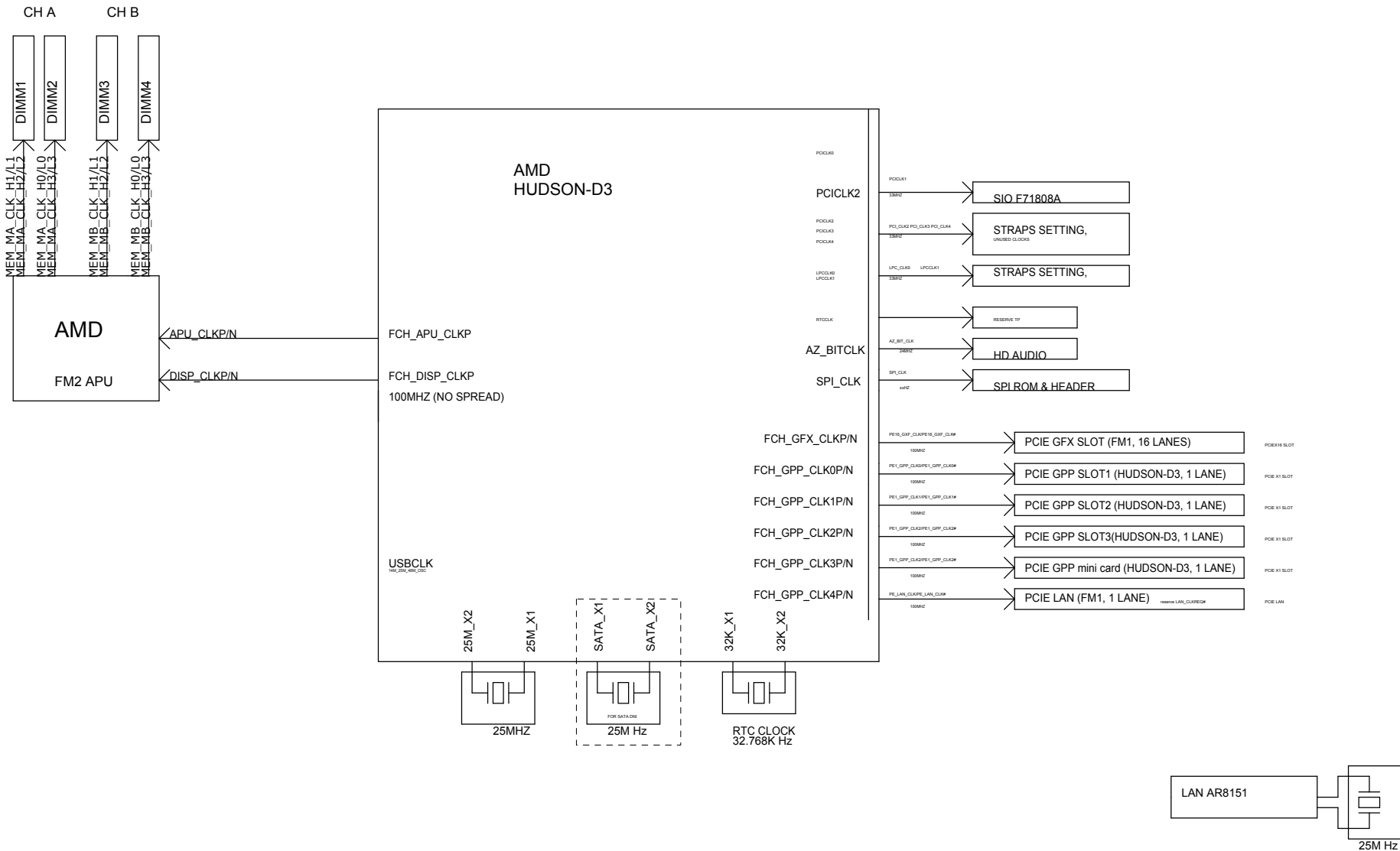
Date:

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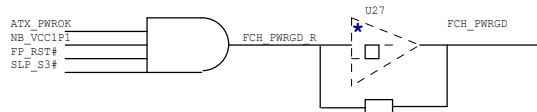
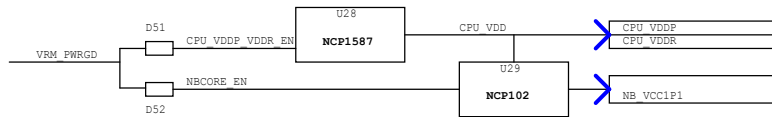
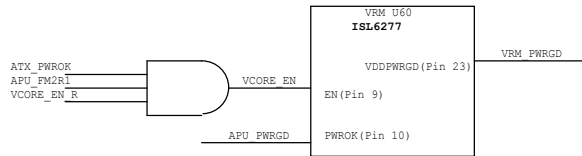
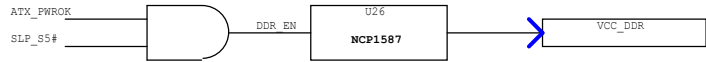
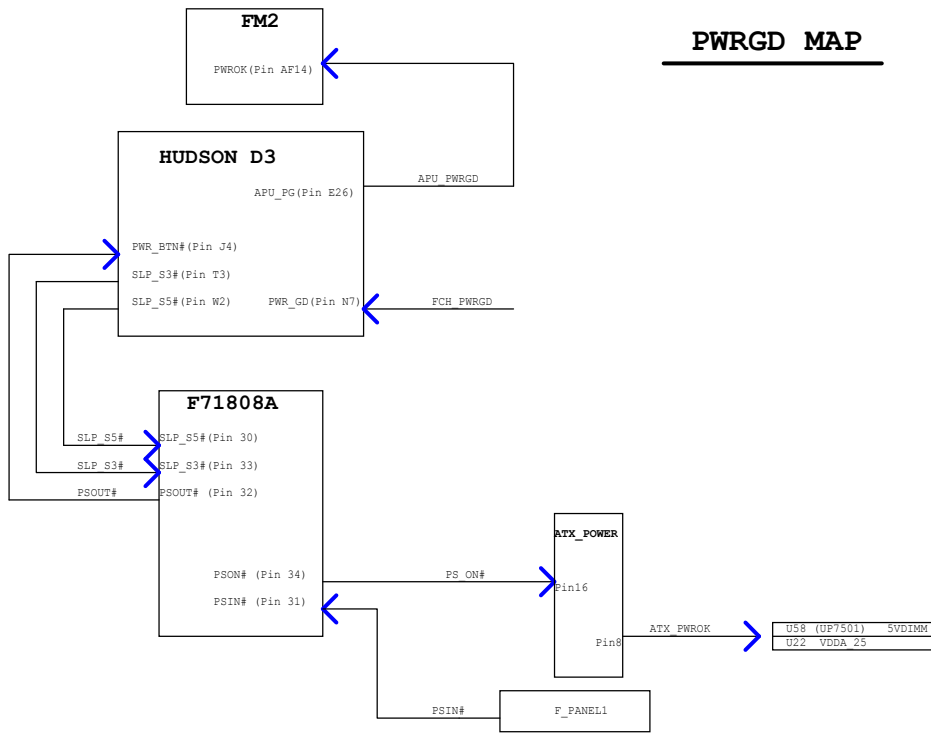
Power Deliver Chart



INTERNAL CLOCK MODE

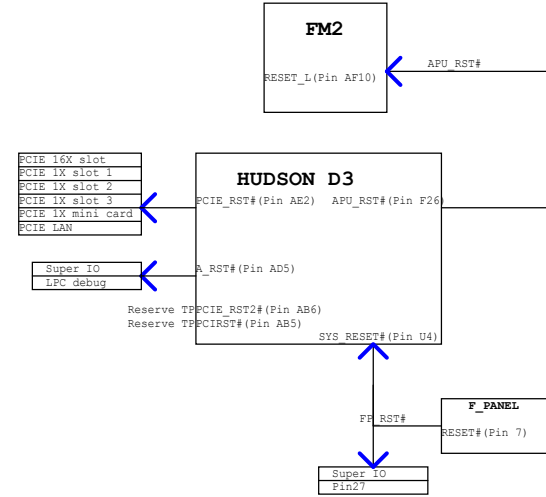


PWRGD MAP



- * - MEANS OPTION

RESET MAP



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PWRGD&RESET Map

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Date:

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SUPER I/O F71808A GPIO Config

Pin	GPIO	Power Rail	Function description	Comment
20	GP22	VSB	POP_MUTE	
22	LEDVSB/GP24	VSB	LED1	
23	LEDVCC/GP25	VSB	LED_SW	
26	GP67	VSB	DEEP_S5	
53	GP00	VSB	EN_LD	
54	GP01	VSB	EN_HP	
55	GP02	VSB	EN_UVP	
58	GP05	VSB	FDO	
60	GP07	VSB	F_AUDIO_DET#	

FCH HUDSON D3 GPIO Config

Name	Pin	Function Description
GPIO0	AJ3	CLEAR CMOS
GPIO1	AL5	WLAN PWRON
GPIO2	AG4	USB20F1A
GPIO3	AL6	USB20F1B
GPIO4	AH3	USB20F2A
GPIO5	AJ5	USB20F2B
GPIO6	AL1	USB20F3
GPIO7	AN5	USB30FA
GPIO8	AN6	USB30FB
GPIO12	AM7	HW_ID1
GPIO13	AJ6	HW_ID2
GPIO14	AK7	HW_ID3
GPIO15	AN8	HW_ID4
GPIO23	AE21	STRAPPING
GPIO24	AC12	STRAPPING
GPIO25	AE13	STRAPPING
GPIO26	AF13	STRAPPING
GPIO27	AH13	STRAPPING
GPIO36	AF1	STRAPPING
GPIO38	AG2	STRAPPING
GPIO39	AF6	STRAPPING
GPIO42	AM17	STRAPPING
GPIO43	AD26	SMBus Clock 0
GPIO46	AK17	STRAPPING
GPIO47	AD25	SMBus Data 0
GPIO52	AH16	STRAPPING
GPIO67	AD22	SATA_LED
GPIO162	V3	SPI Clock
GPIO163	V5	SPI Data Out
GPIO164	V6	SPI Data In
GPIO165	T6	SPI Chip Select 1
GPIO170	Y1	HD Audio Serial Data
GPIO181	M1	LAN_ISOLATEB
GPIO199	J22	STRAPPING

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1 CH-A	10100000B A0H	MEM_MA_CLK_H1/L1 MEM_MA_CLK_H2/L2
DIMM 2 CH-A	10100010B A4H	MEM_MA_CLK_H0/L0 MEM_MA_CLK_H3/L3
DIMM 3 CH-B	10100001B A2H	MEM_MB_CLK_H1/L1 MEM_MB_CLK_H2/L2
DIMM 4 CH-B	10100011B A6H	MEM_MB_CLK_H0/L0 MEM_MB_CLK_H3/L3

SMBus TABLE

SOURCE	SINGLE NAME	LINKED DEVICE
APU	DP0_AUXP_C /DP0_AUXN_C	DVI
	DP1_AUXP_C /DP1_AUXN_C	Hudson D3 DP to VGA translator
FCH	SCLK0/SDATA0	DIMMs,CLOCK GEN ,SIO
	SCLK1/SDATA1	LAN,PCIE SLOTS,MINI_PCIE
	SCLK3/SDATA3	TP

RESET TABLE

SOURCE	SINGLE NAME	LINKED DEVICE
FCH	PCIE_RST#	PCie 16X,1X,LAN,MINI_PCIE
	A_RST#	SIO,LPC debug
	PCIE_RST2#	RESERVE TP
	LDT_RST#	APU
	AZ_RST#	AZALIA CODEC
	DDR3_RST#	NC
	FC_RST#	DEBUG BUS
	ROM_RST#	NC
FRONT PANEL	FP_RST#	FCH,CLOCK GEN

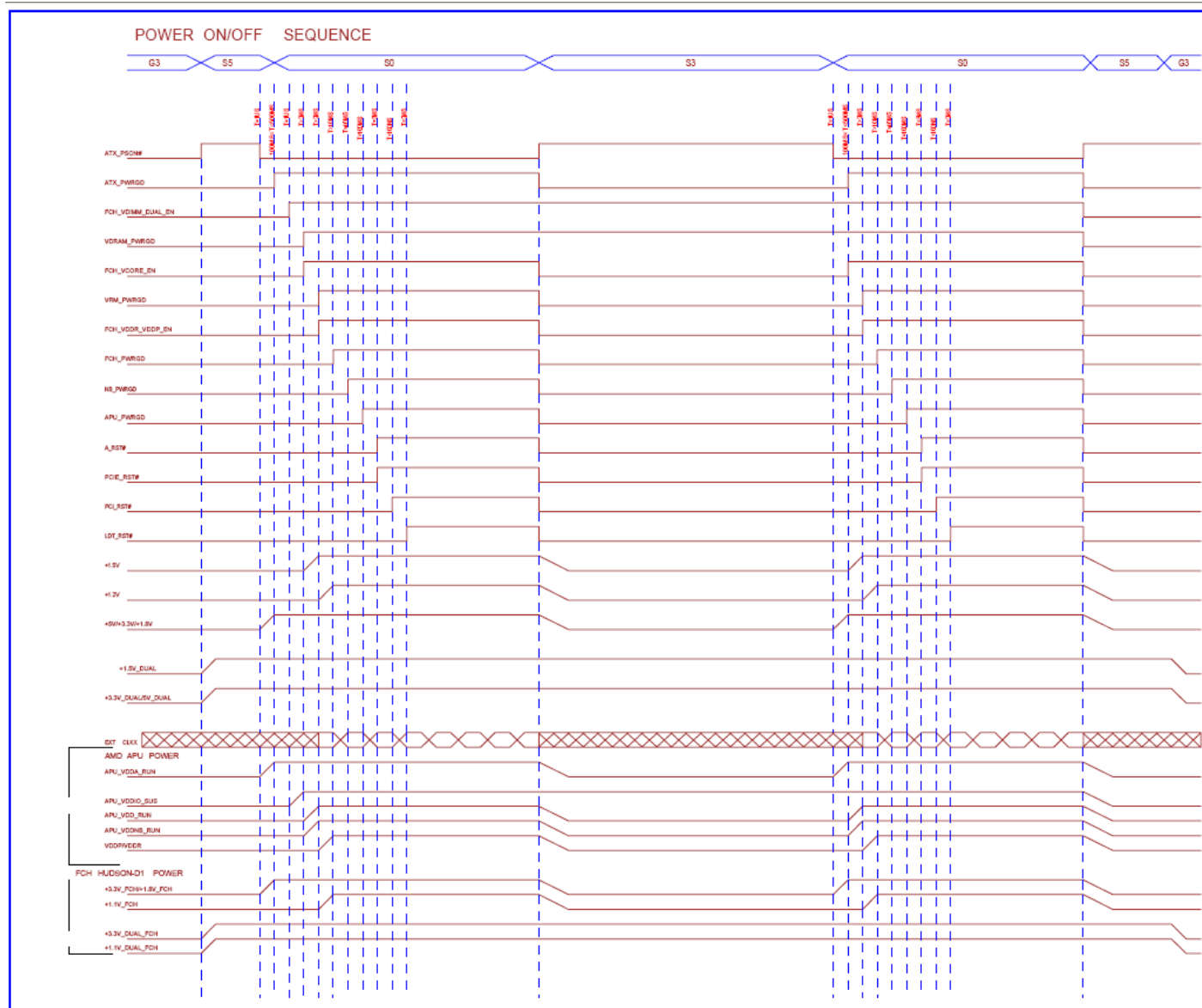


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Date:	Sheet 6 of 45	

POWER ON SEQUENCE



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HP SCH P/N: (MSI MS-7778)

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Document Description

POWER ON SEQUENCE

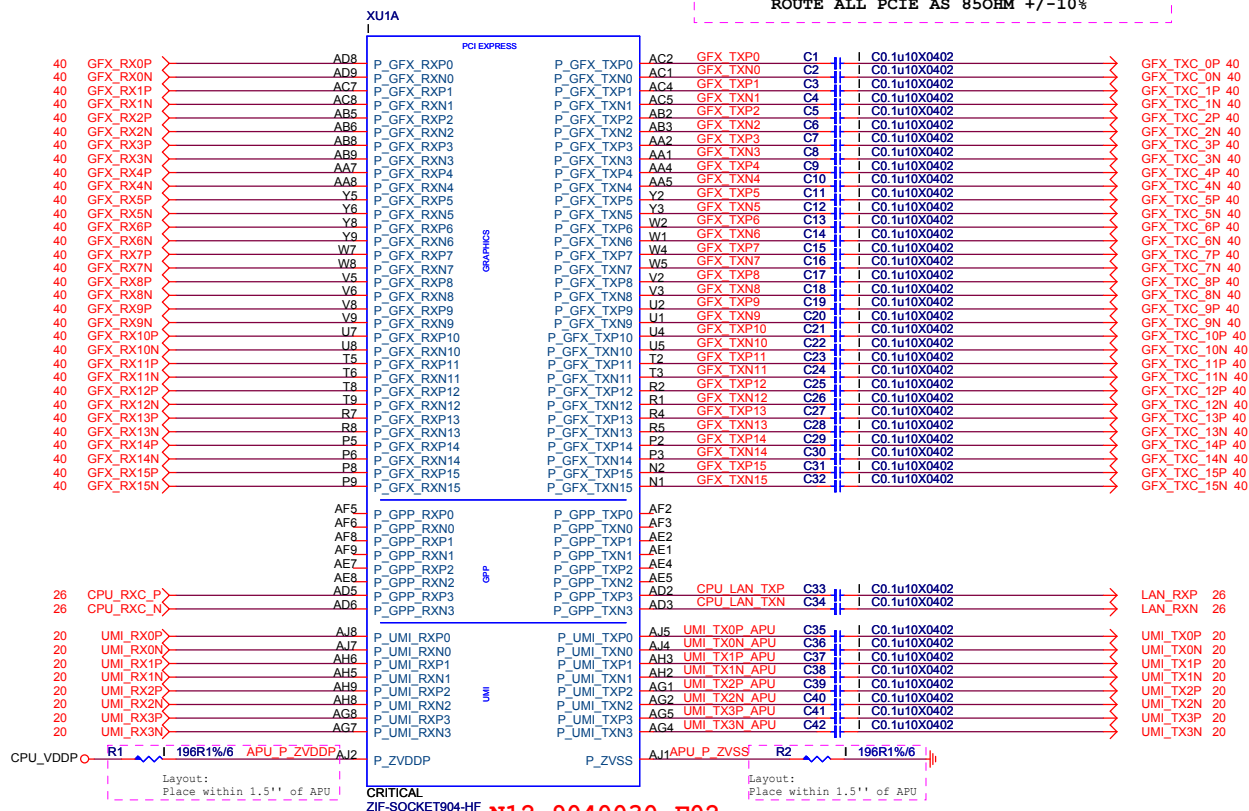
Rev
0A

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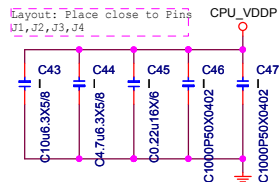
Sheet 7 of 45

FM2 PCIE I/F

mach@CRB PCIE AC Capacitors:75nF to 200nF
Layout: PLACE CAPS WITH APU < 1 INCH
ROUTE ALL PCIE AS 85OHM +/-10%



CRITICAL
ZIF-SOCKET904-HF N12-9040030-F02

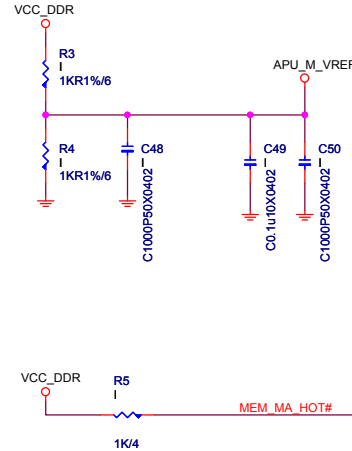


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HP SCH P/N: (MSI MS-7778)

Size	Document Description	Rev
Custom	FM2 PCIE I/F	0A
Date:	Sheet 8 of 45	

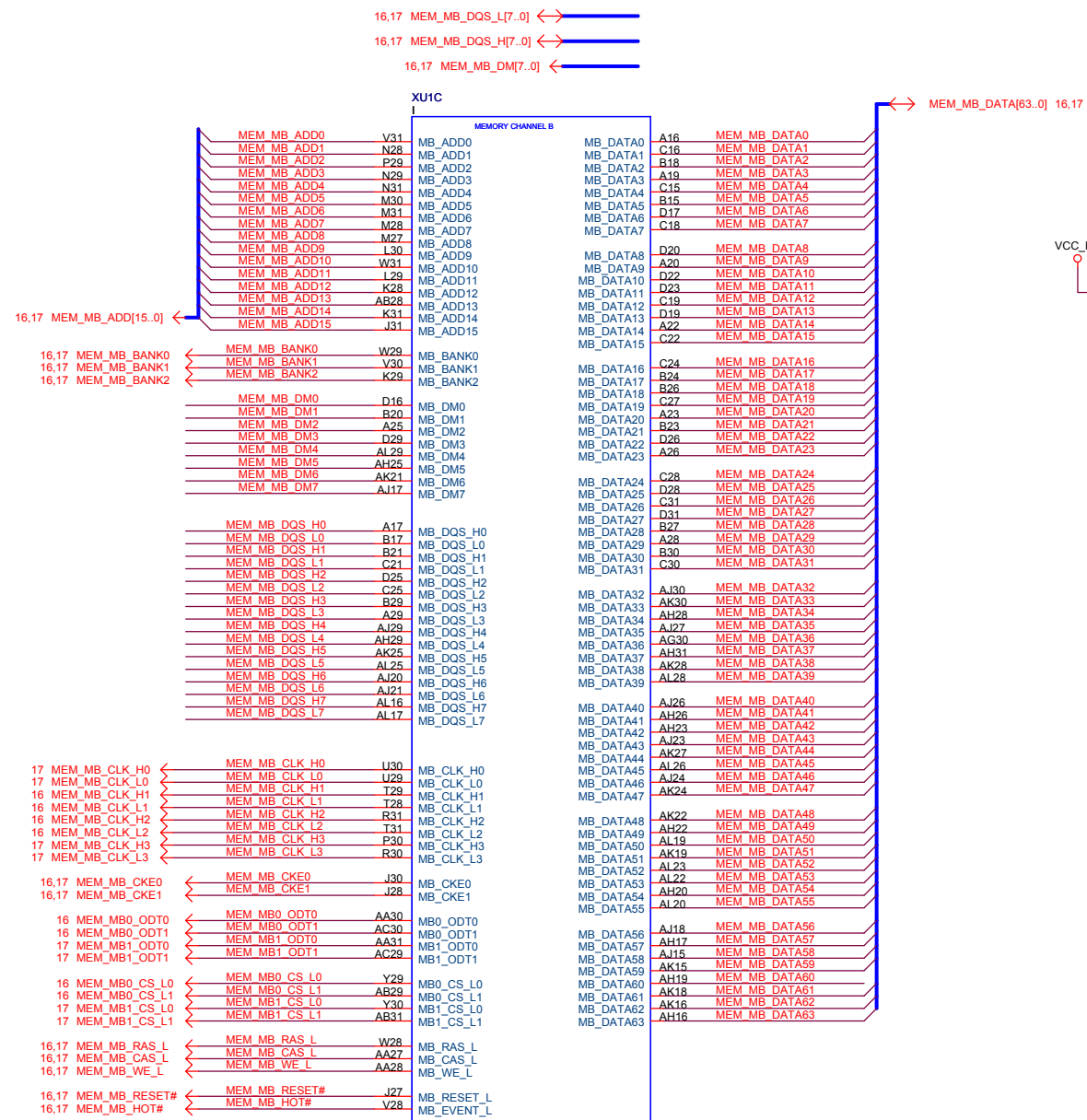
14,15 MEM_MA_DQS_L[7..0] <-->
14,15 MEM_MA_DQS_H[7..0] <-->
14,15 MEM_MA_DM[7..0] <-->



CRITICAL
ZIF-SOCKET904-HF N12-9040030-F02



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HP SCH P/N: (MSI MS-7778)		
Size Custom	Document Description	Rev 0A
FM2 DDR3 I/F(A)		
Date:	Sheet 9 of 45	



CRITICAL

ZIF-SOCKET904-HF

N12-9040030-F02



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HP SCH P/N: (MSI MS-7778)		
Size Custom	Document Description	Rev 0A
FM2 DDR3 I/F(B)		
Date:	Sheet 10 of 45	

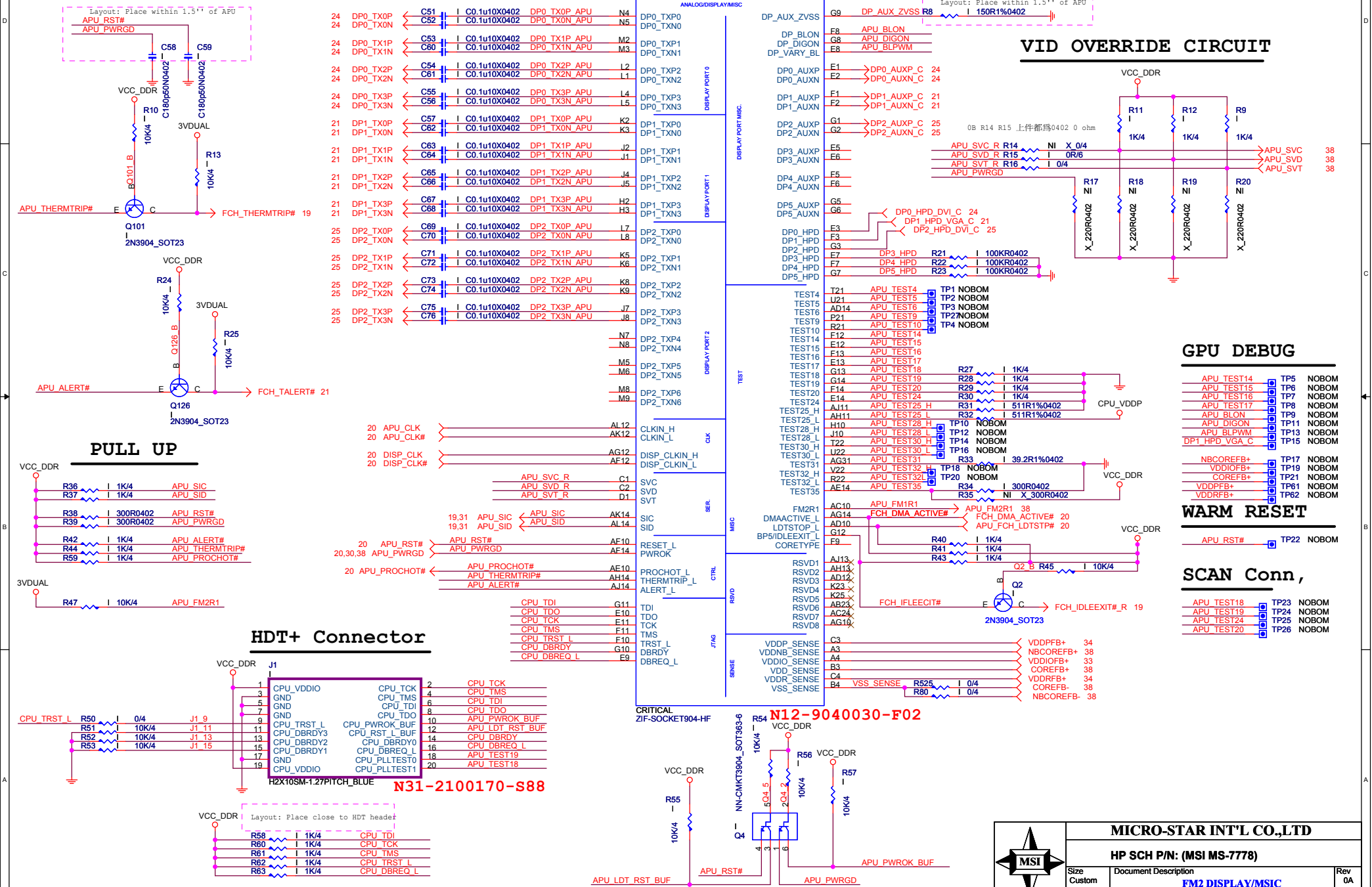
FM1 DISPLAY I/F

Note: Several vias on the DP0 interface violate the minimum distance rules for via to via spacing between diff pairs. These violations have been reviewed and approved on an individual basis, and pose no significant signal integrity issues for this implementation since the route lengths are under the maximum allowed spec, and the via distance violations are not severe.

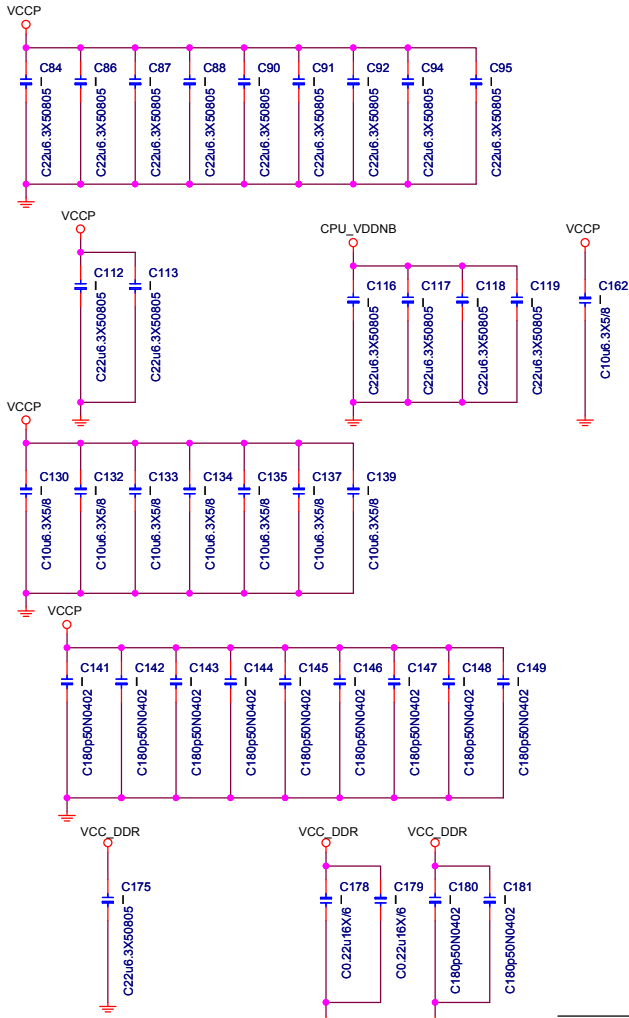
ROUTE PCIE AS 850HM +/-10%

PLACE CAPS WITH APU < 1 INCH

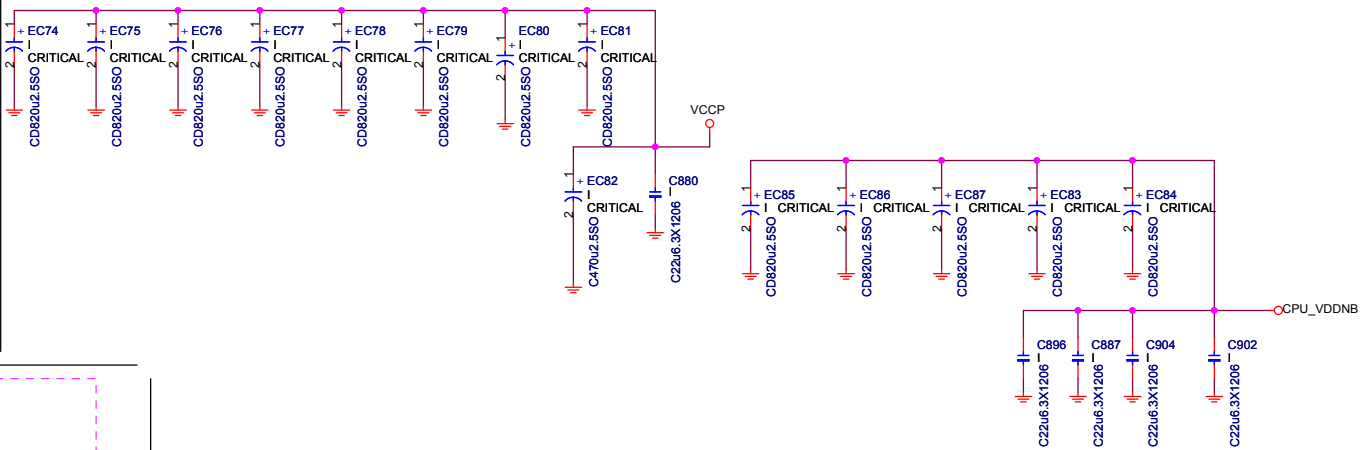
Trace length within 10"



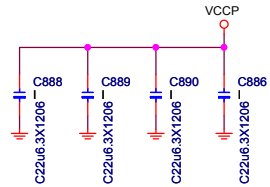
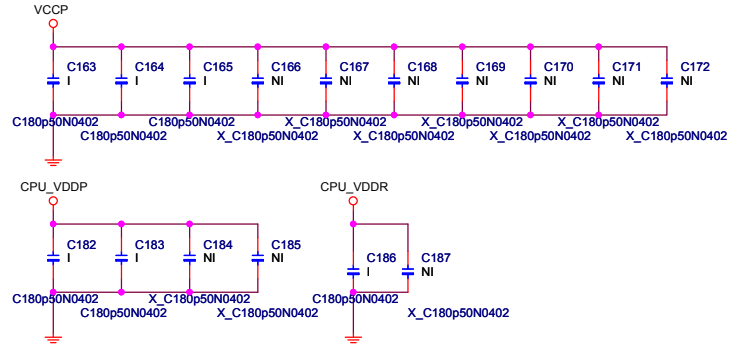
CPU POWER CAPS



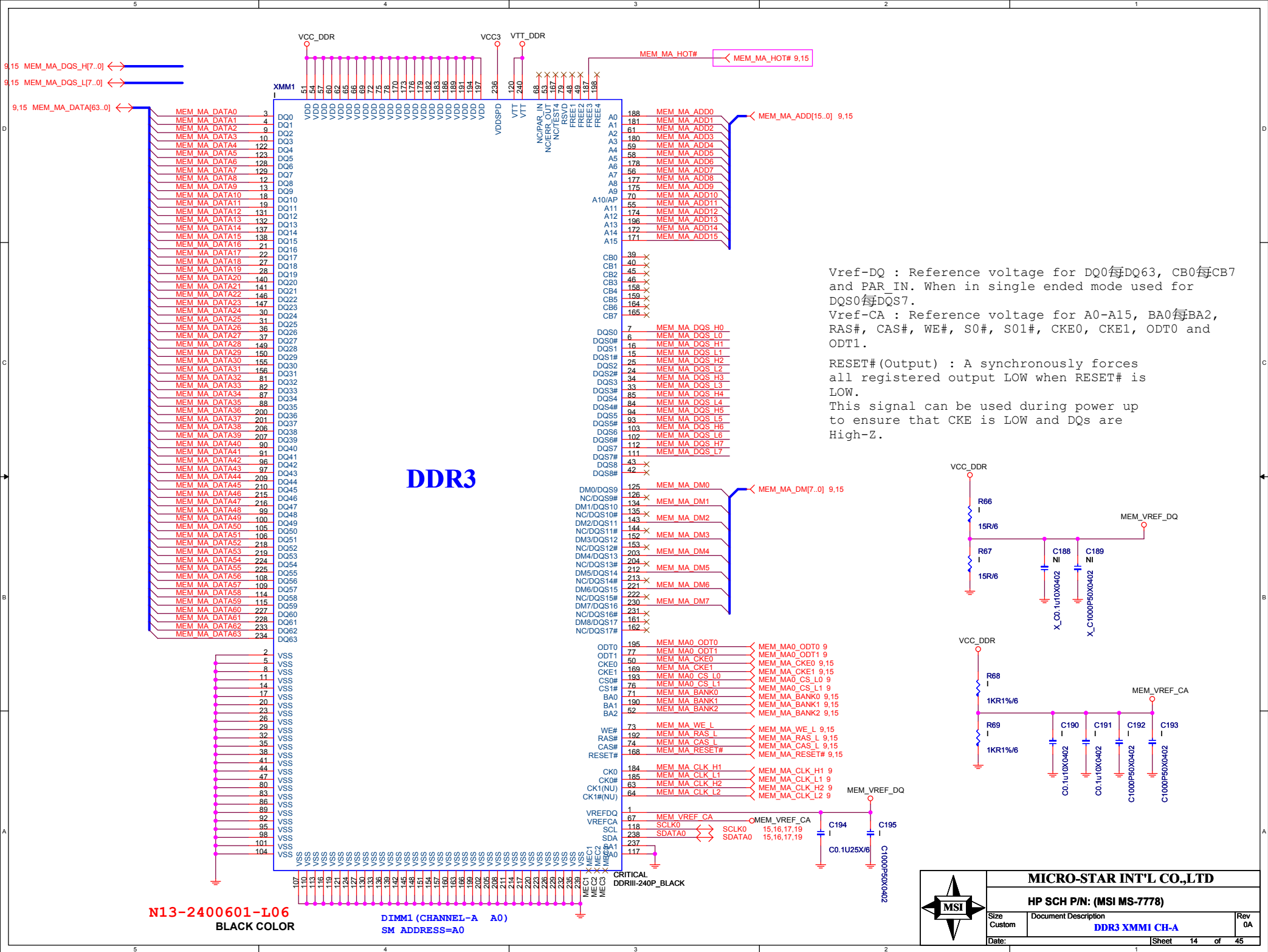
VCORE CAPS



EMC Caps On Bottom side



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Size Custom	Document Description FM2 CAPS & VCORE CAP	Rev 0A
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DDR3

N13-2400921-L06
BLUE COLOR

DIMM2 (CHANNEL-A A1)
SM ADDRESS=A4



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Custom

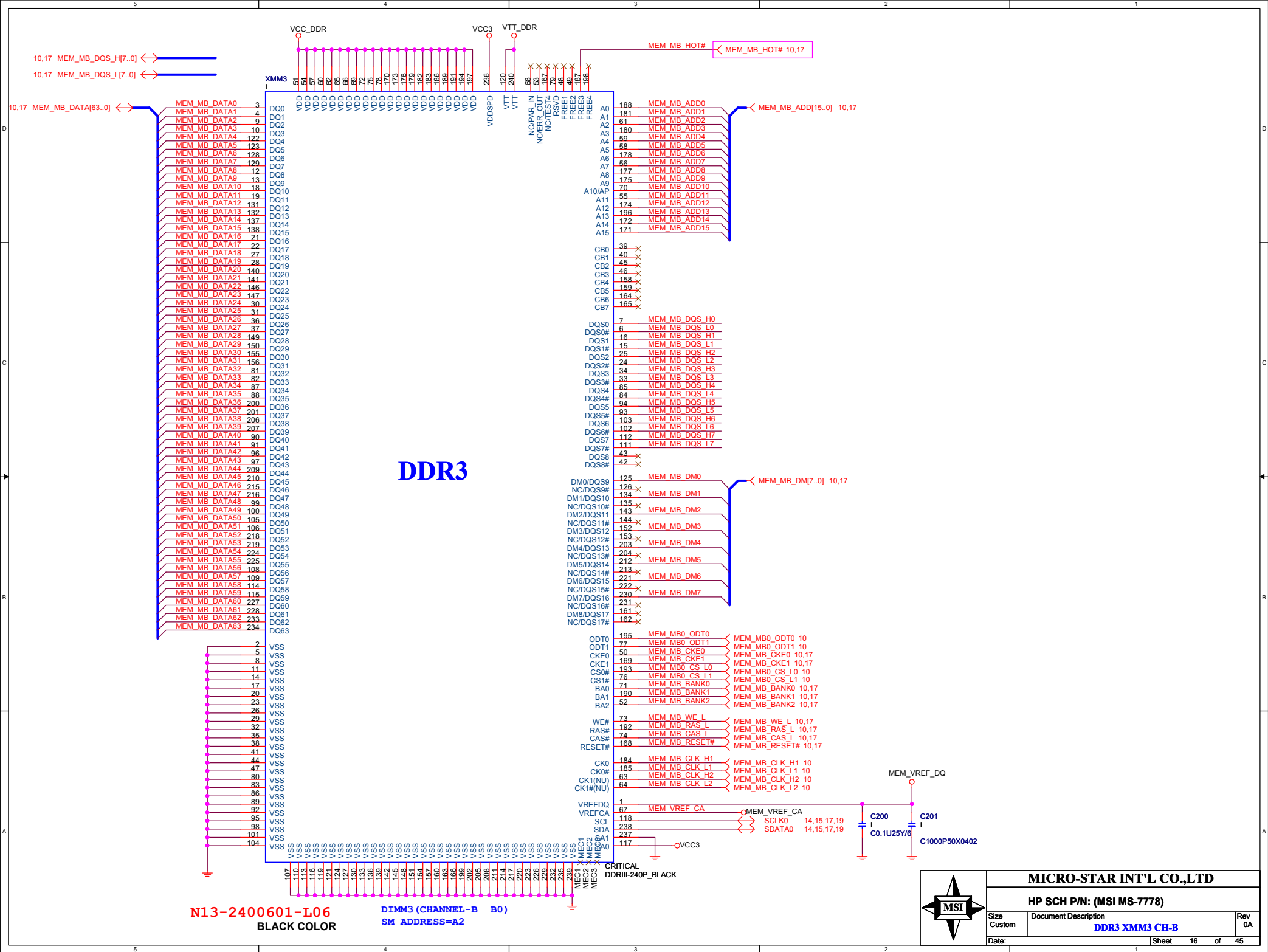
Document Description

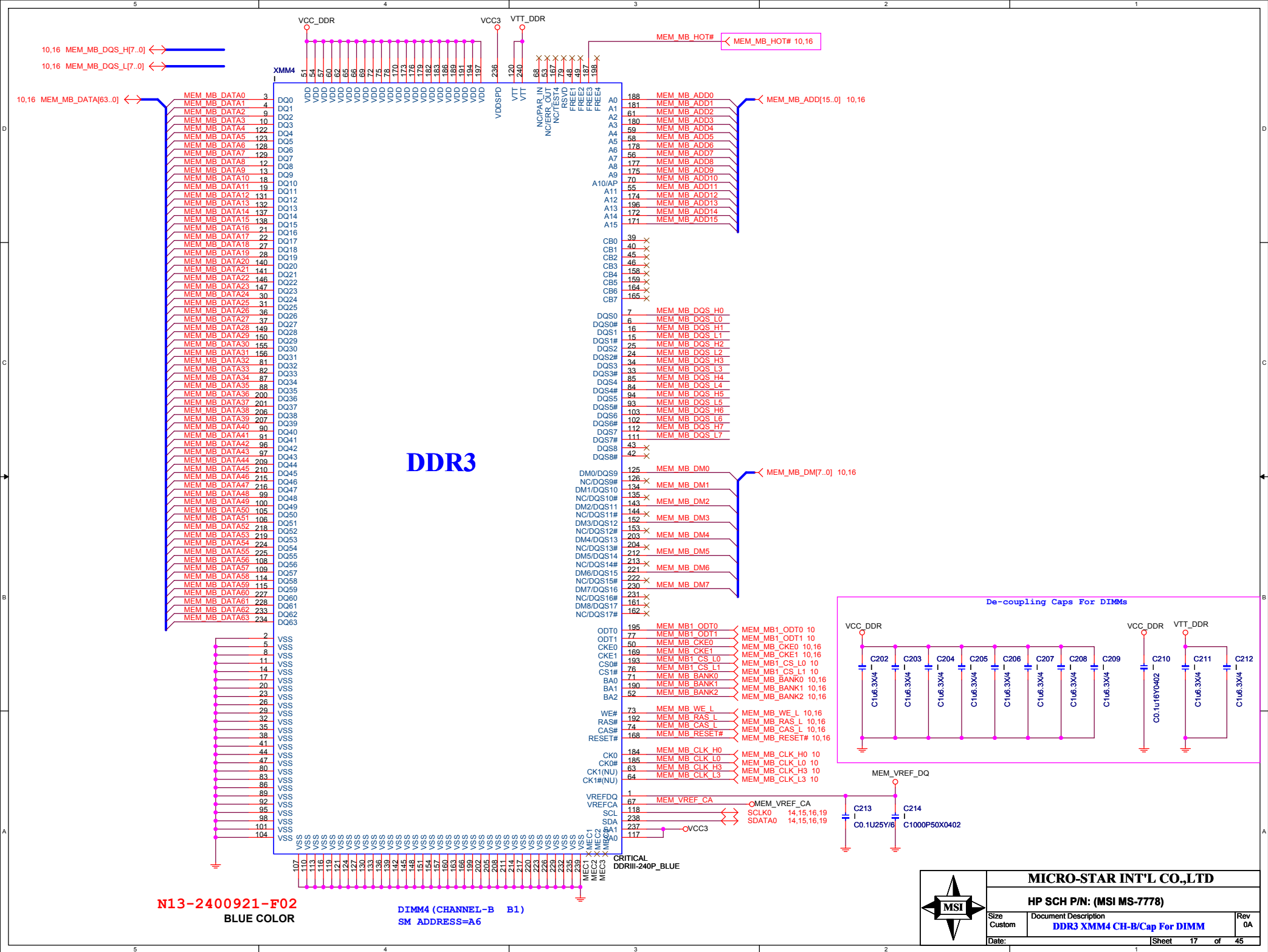
DDR3 XMM2 CH-A

Rev
0A

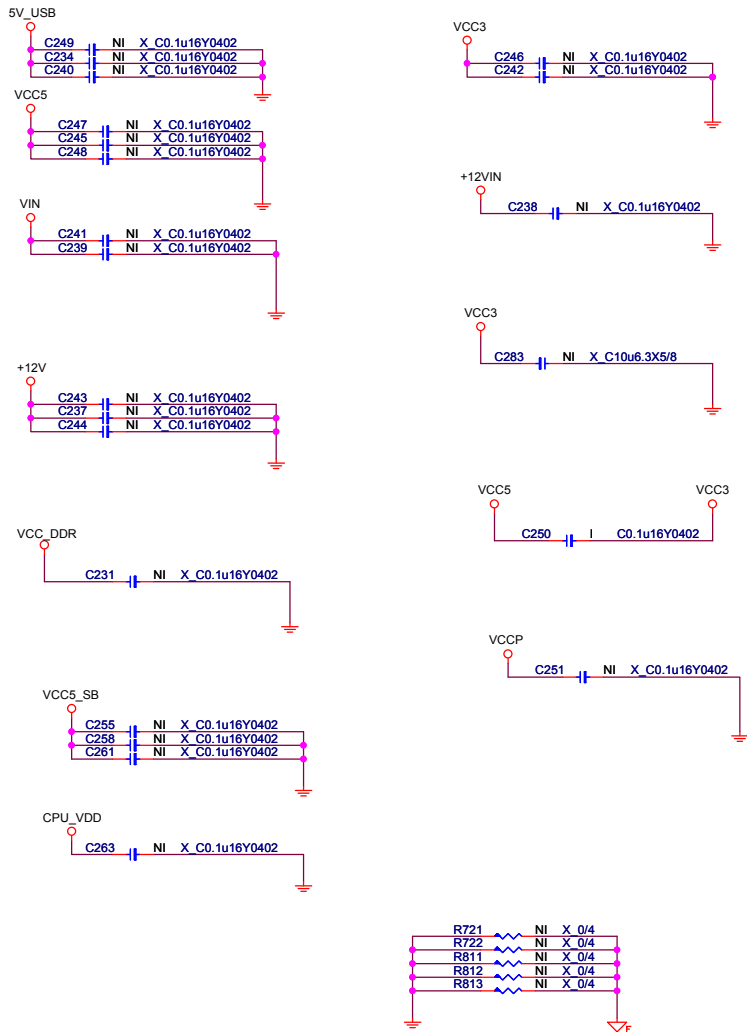
Date:

Sheet 15 of 45



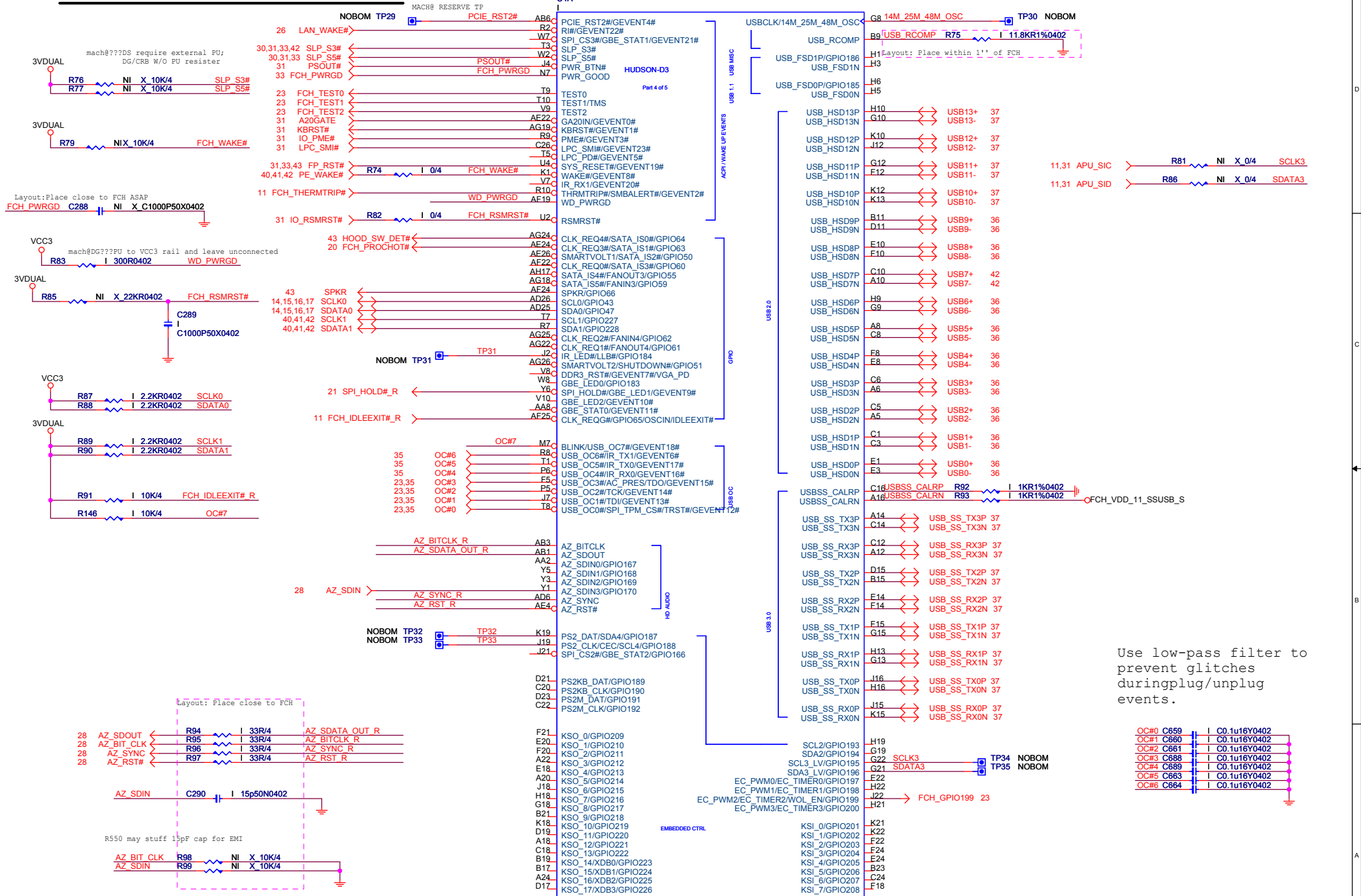


EMI Reserved

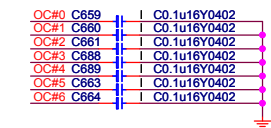


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HUDSON ACPI/USB/AZ/GPIO



Use low-pass filter to prevent glitches during plug/unplug events.



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HUDSON ACPI/USB/AZ/GPIO

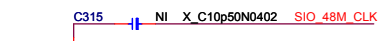
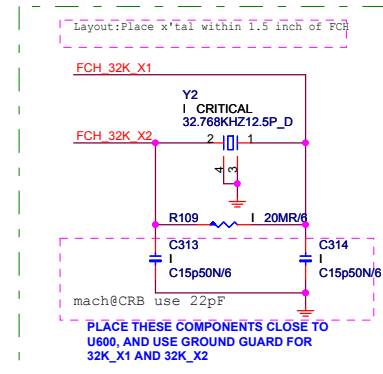
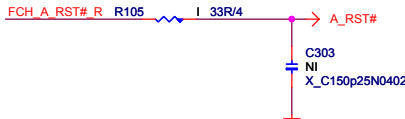
Size
Custom
Date:

Rev	0A
-----	----

Sheet 19 of 45

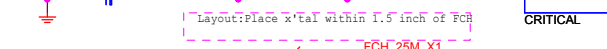
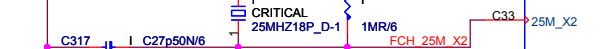
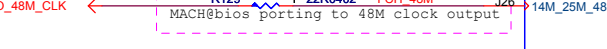
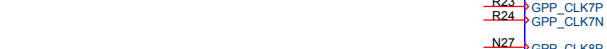
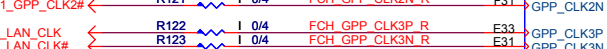
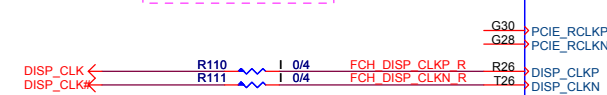
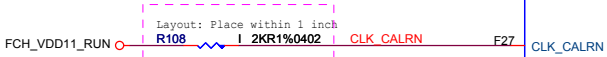
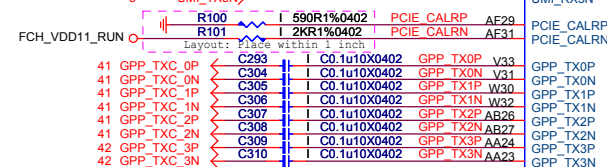
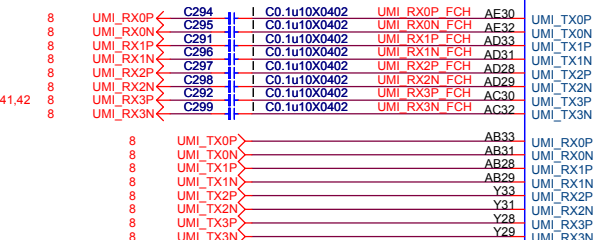
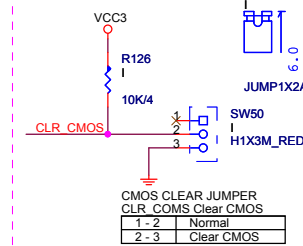
HUDSON PCIE/PCI/APU/LPC/CLK

A_RST# for LPC device;
PCIE_RST# for APU PCIE device;
PCIE_RST#2 FCH PCIE device

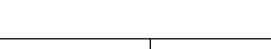
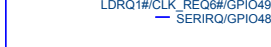
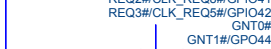
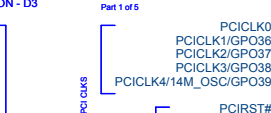


CLEAR CMOS

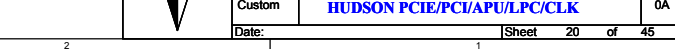
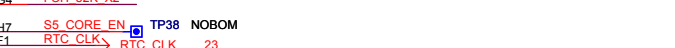
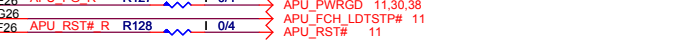
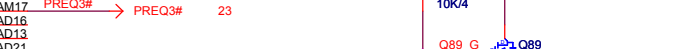
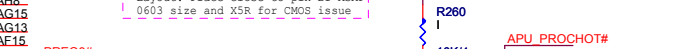
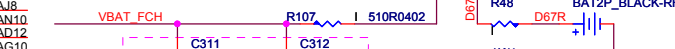
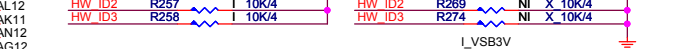
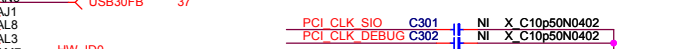
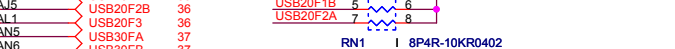
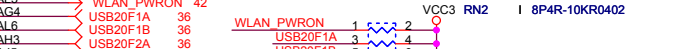
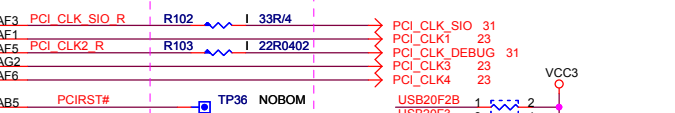
N31-1030211-H06



HUDSON - D3



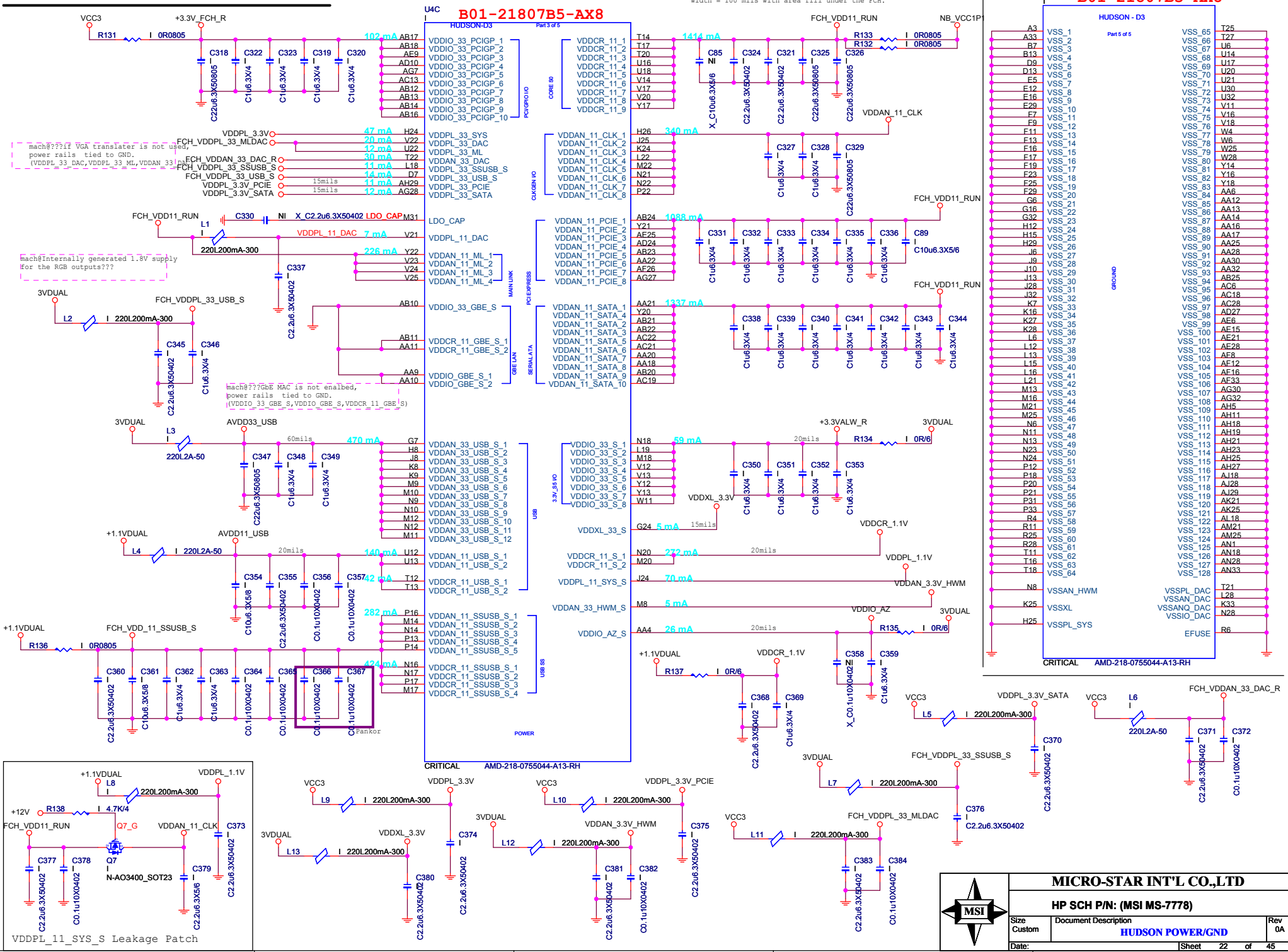
Part 1 of 5



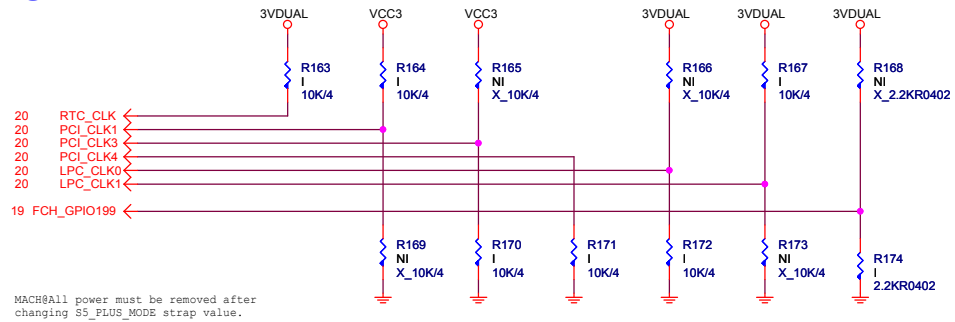
MICRO-STAR INT'L CO.,LTD		
HP SCH P/N: (MSI MS-7778)		
Size	Document Description	Rev
Custom	HUDSON PCIE/PCI/APU/LPC/CLK	0A
Date:	Sheet	of
	20	45

B01-21807B5-AX8

HUDSON POWER&DECOUPLING



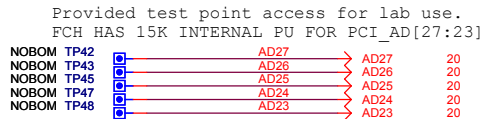
FCH REQUIRED STRAPS



MACH#All power must be removed after changing S5_PLUS_MODE strap value.

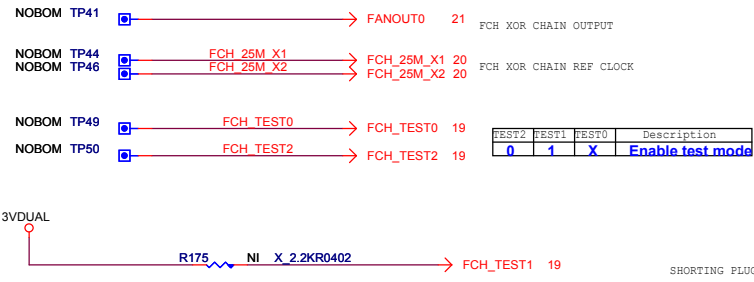
	RTCCLK	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO199
PULL HIGH	S5 PLUS MODE DISABLED DEFAULT	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	Reserved	EC ENABLED	INTERNAL CLOCK GEN ENABLED DEFAULT	LPC ROM
PULL LOW	S5 PLUS MODE ENABLED	FORCE PCIE GEN1	IGNORE DEBUG STRAPS DEFAULT	Required setting for intergrated CLOCK MODE DEFAULT	EC DISABLED DEFAULT	INTERNAL CLOCK GEN DISABLED	SPI ROM DEFAULT

FCH DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	RESERVED	Normal REFCLK Termination DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL DOWN	BYPASS PCI PLL	RESERVED	Inverted REFCLK Termination	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

FCH XOR CHAIN TEST

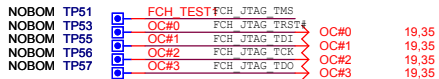


TEST2	TEST1	TEST0	Description
0	1	X	Enable test mode

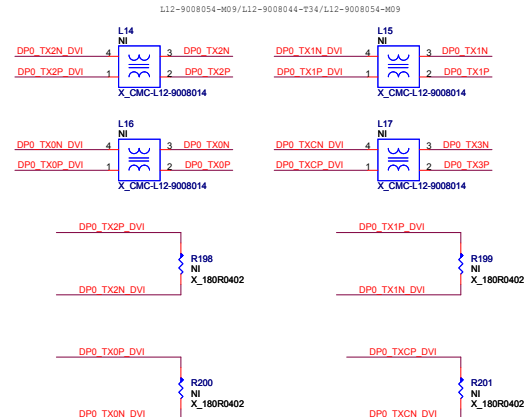
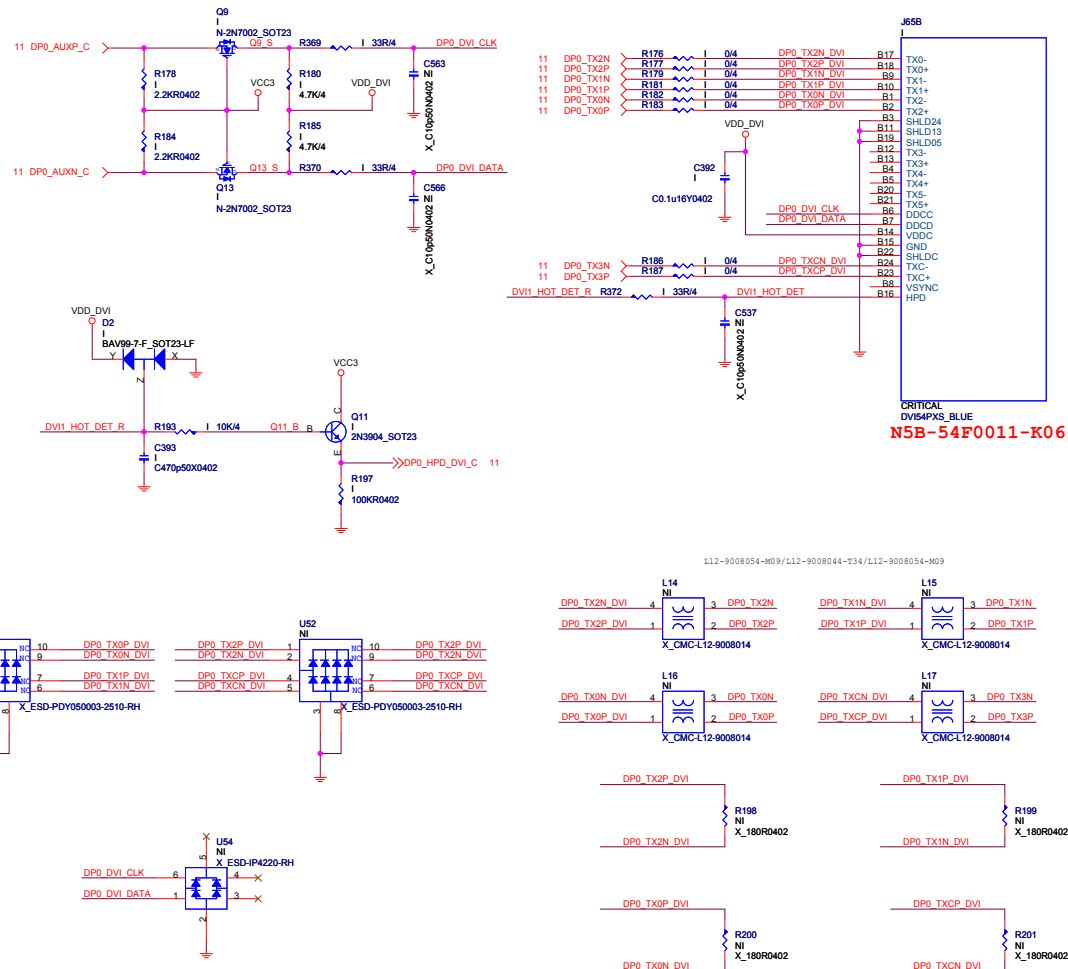
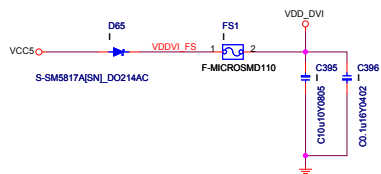
FCH PCIE EEPROM STRAPS



FCH ICE DEBUG /JTAG TEST PINS



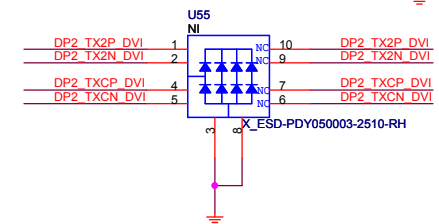
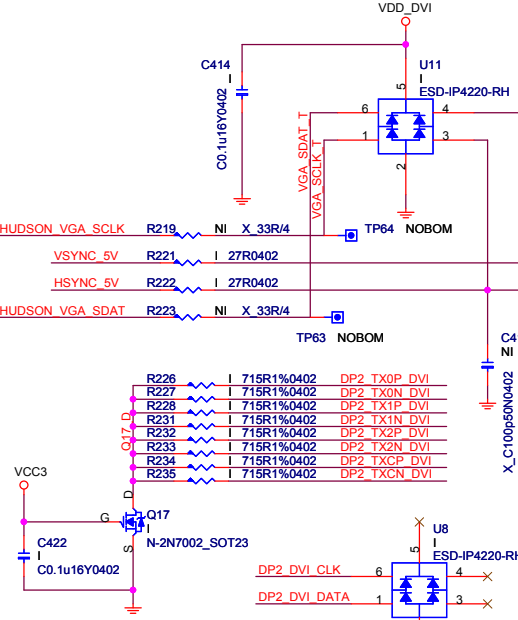
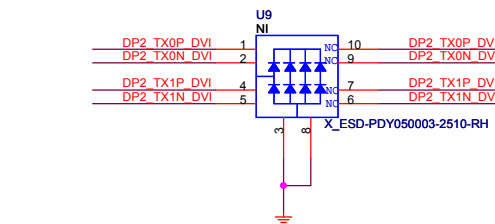
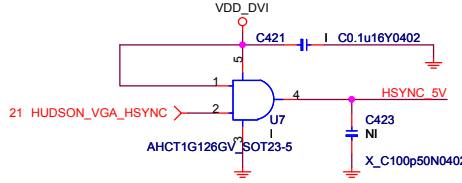
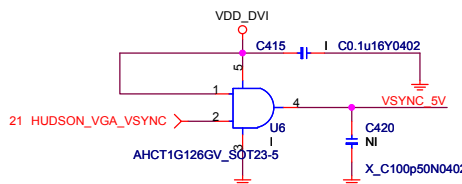
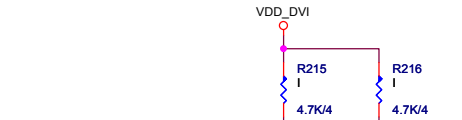
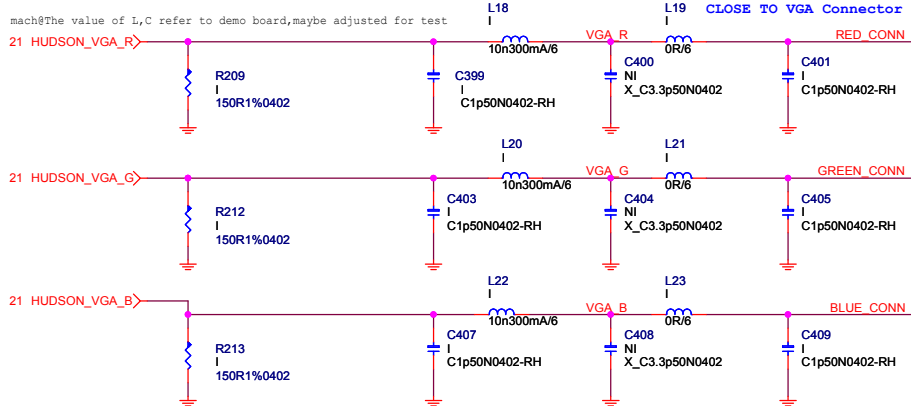
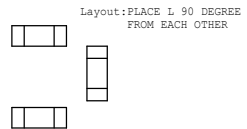
DVI POWER



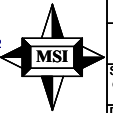
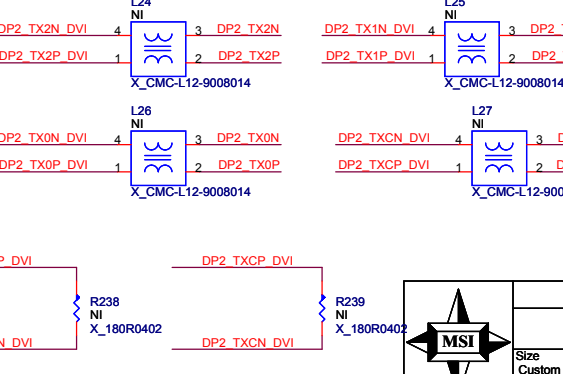
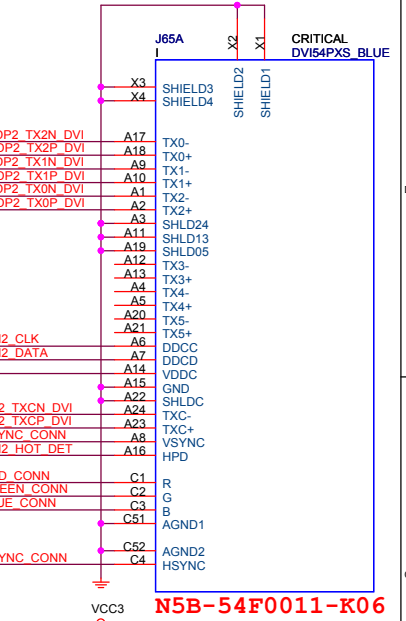
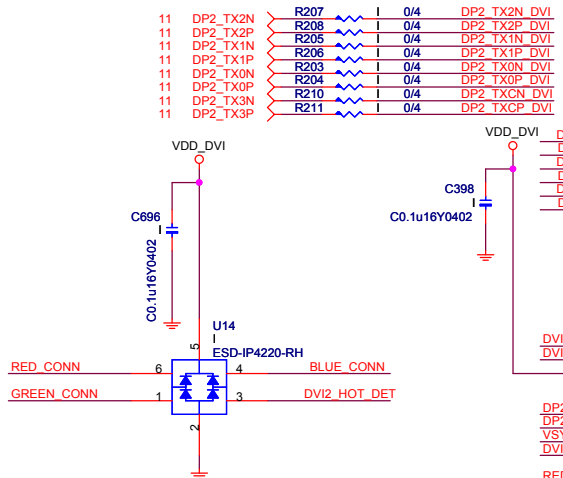
MICRO-STAR INT'L CO.,LTD				
HP SCH P/N: (MSI MS-7778)				
Size C	Document Description DVII CONN.			Rev 0A
Part No.	1 Sheet	2 of	4 of	

DVI2 CONNECTOR

R932-R934 CLOSE TO CRT CONNECTOR, THE TRACE IMPEDANCE BETWEEN NB AND 150OHM
RESISTOR SHOULD BE 37OHM+/-15%, THE TRACE IMPEDANCE BETWEEN THE 2 150OHM
RESISTOR SHOULD BE 50 OHM +/-15%
THE IMPEDANCE BETWEEN THE 2ND RESISTOR TO THE CONNECTOR SHOULD BE 75OHM+/-15%



PLACE ESD PROTECTION DIODES
1. CLOSE TO CONNECTOR PINS
2. DIRECTLY ON SIGNAL TRACES
3. +5V & GND TRACE TO DIODE SHOULD BE LESS THAN 100MILS AND 20MILS WIDE
4. THE ESD DIODE SHOULD BE THE FIRST DEVICE FROM CONNECTOR

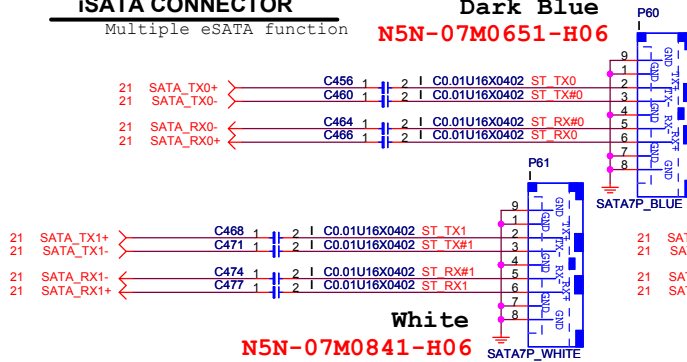


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iSATA CONNECTOR

Multiple eSATA function

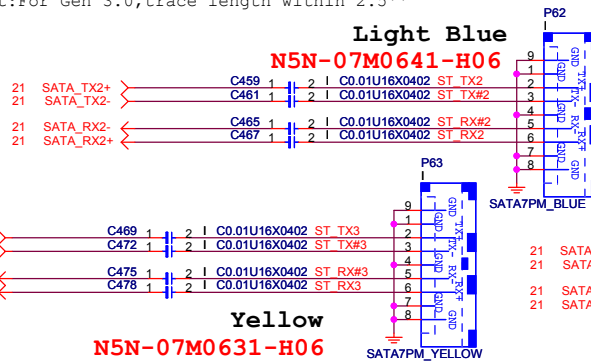
Dark Blue
N5N-07M0651-H06



White
N5N-07M0841-H06

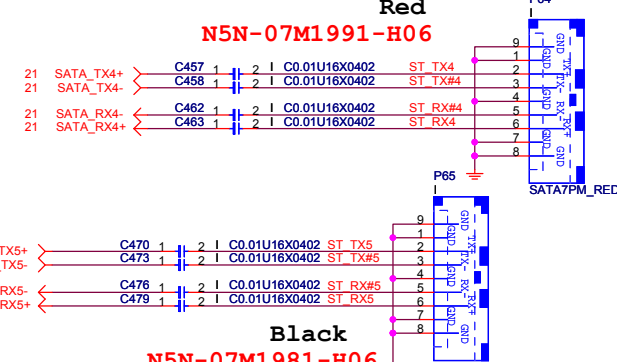
Layout:For Gen 3.0,trace length within 2.5''

Light Blue
N5N-07M0641-H06



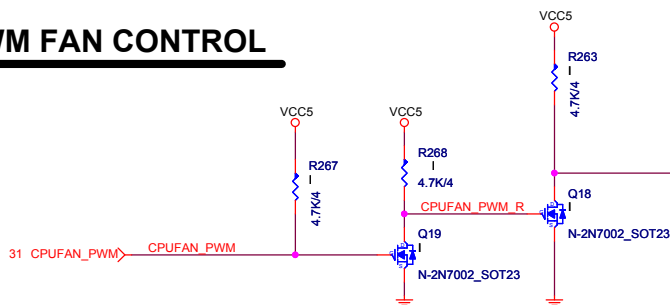
Yellow
N5N-07M0631-H06

Red
N5N-07M1991-H06

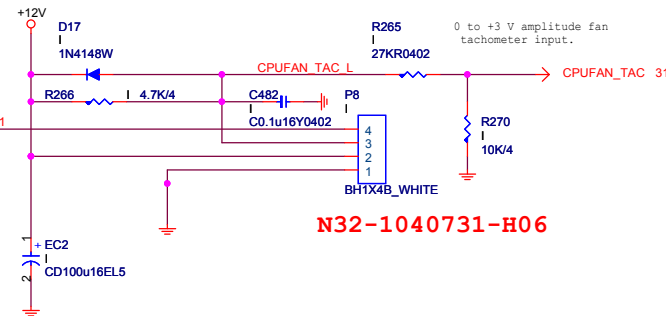


Black
N5N-07M1981-H06

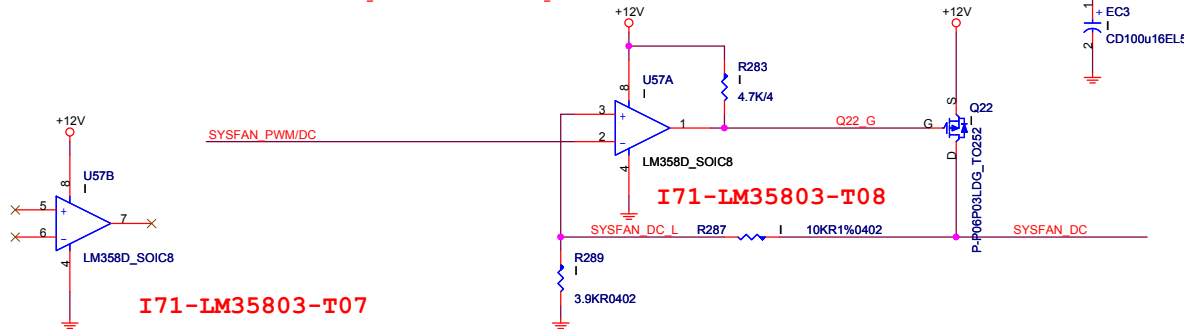
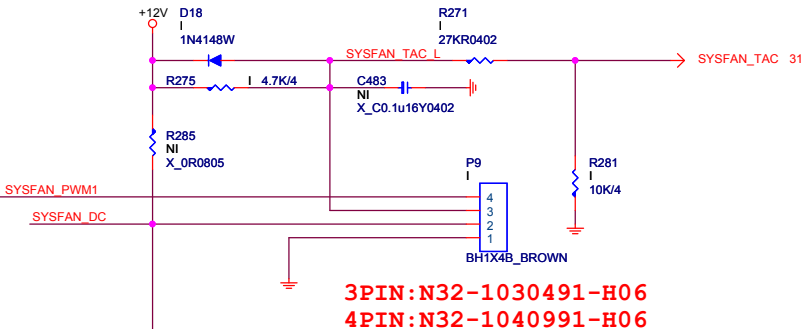
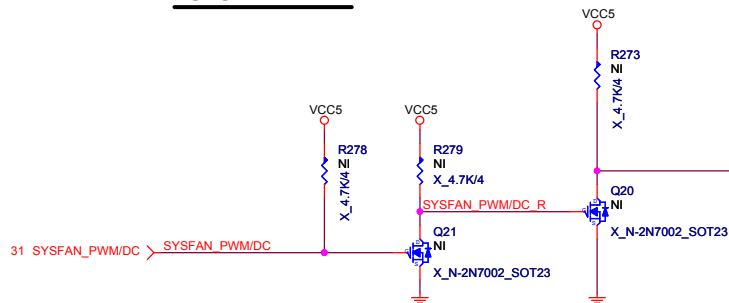
PWM FAN CONTROL



CPU FAN



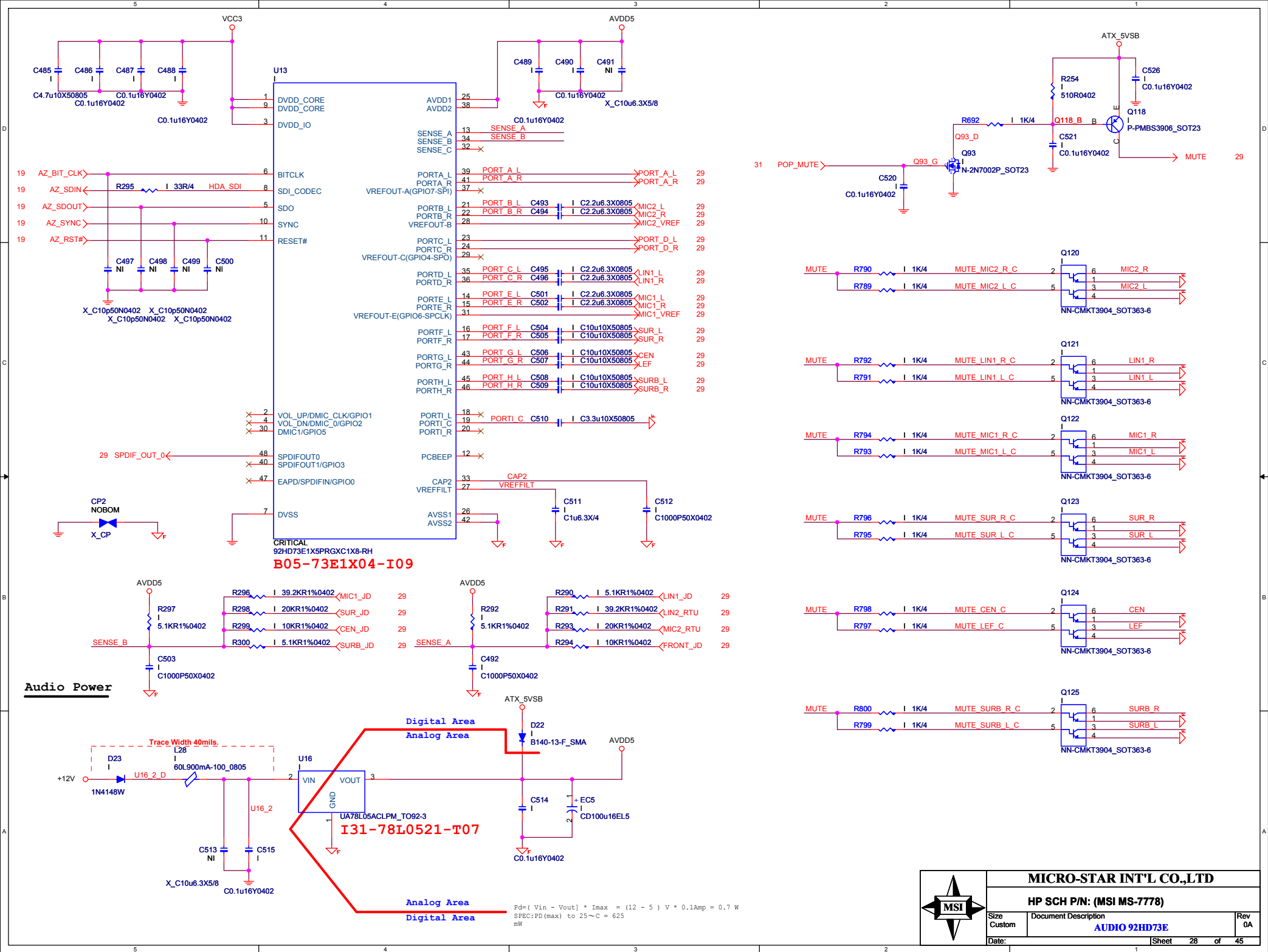
SYSTEM FAN

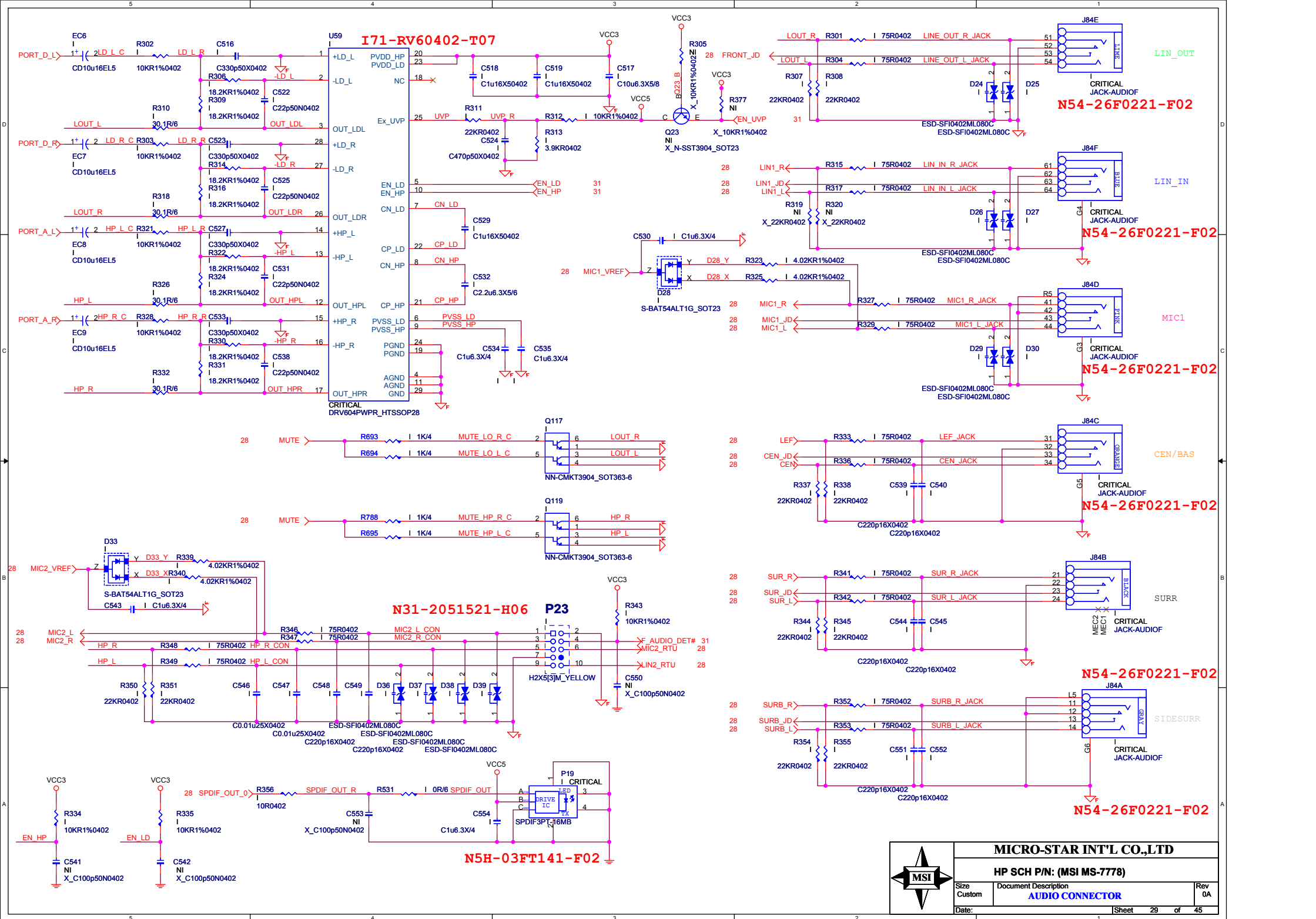


MICRO-STAR INT'L CO.,LTD

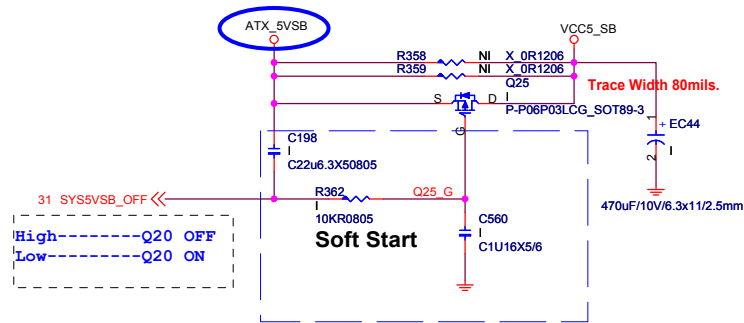
HP SCH P/N: (MSI MS-7778)

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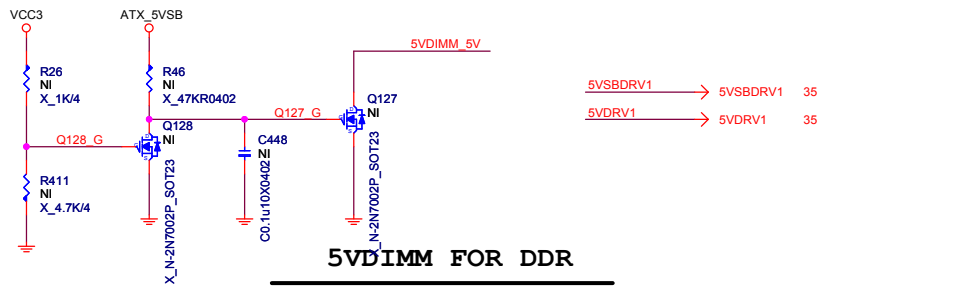




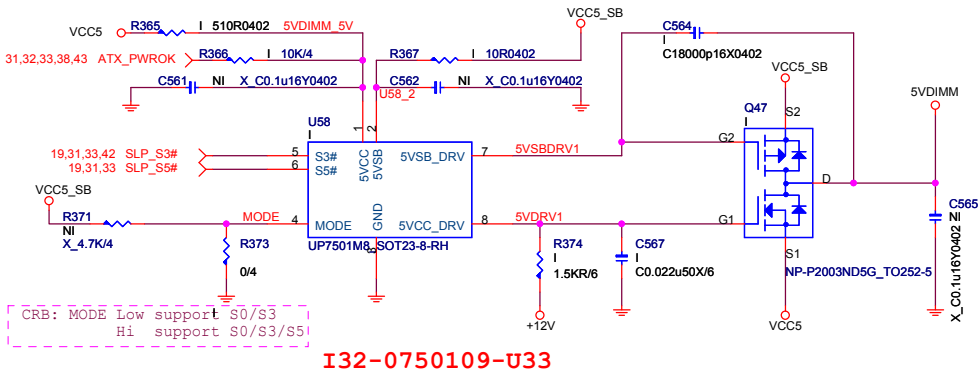
VCC5_SB Power Switch



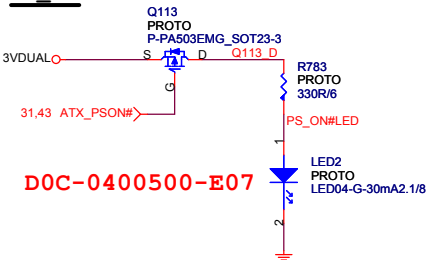
For special PSU sequence



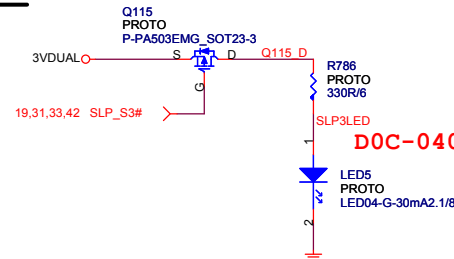
5VIMM FOR DDR



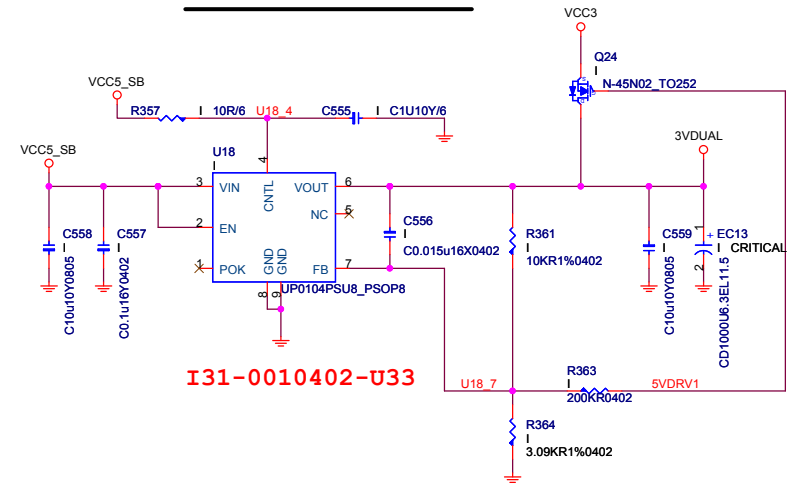
PS_ON#



SLP_S3#

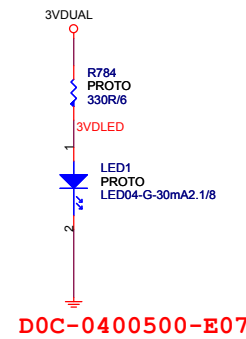


3VDUAL POWER

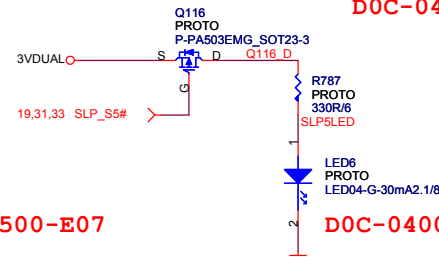


I31-0010402-U33

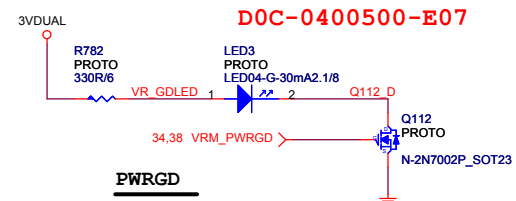
3VDUAL



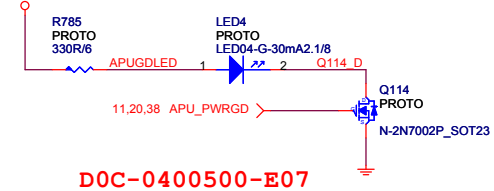
SLP_S5#



VRMPWRGD



PWRGD



DOC-0400500-E07

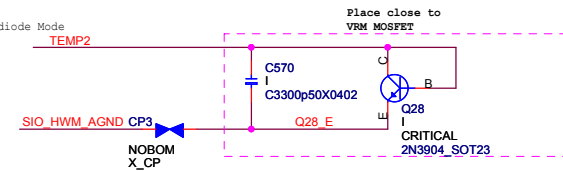
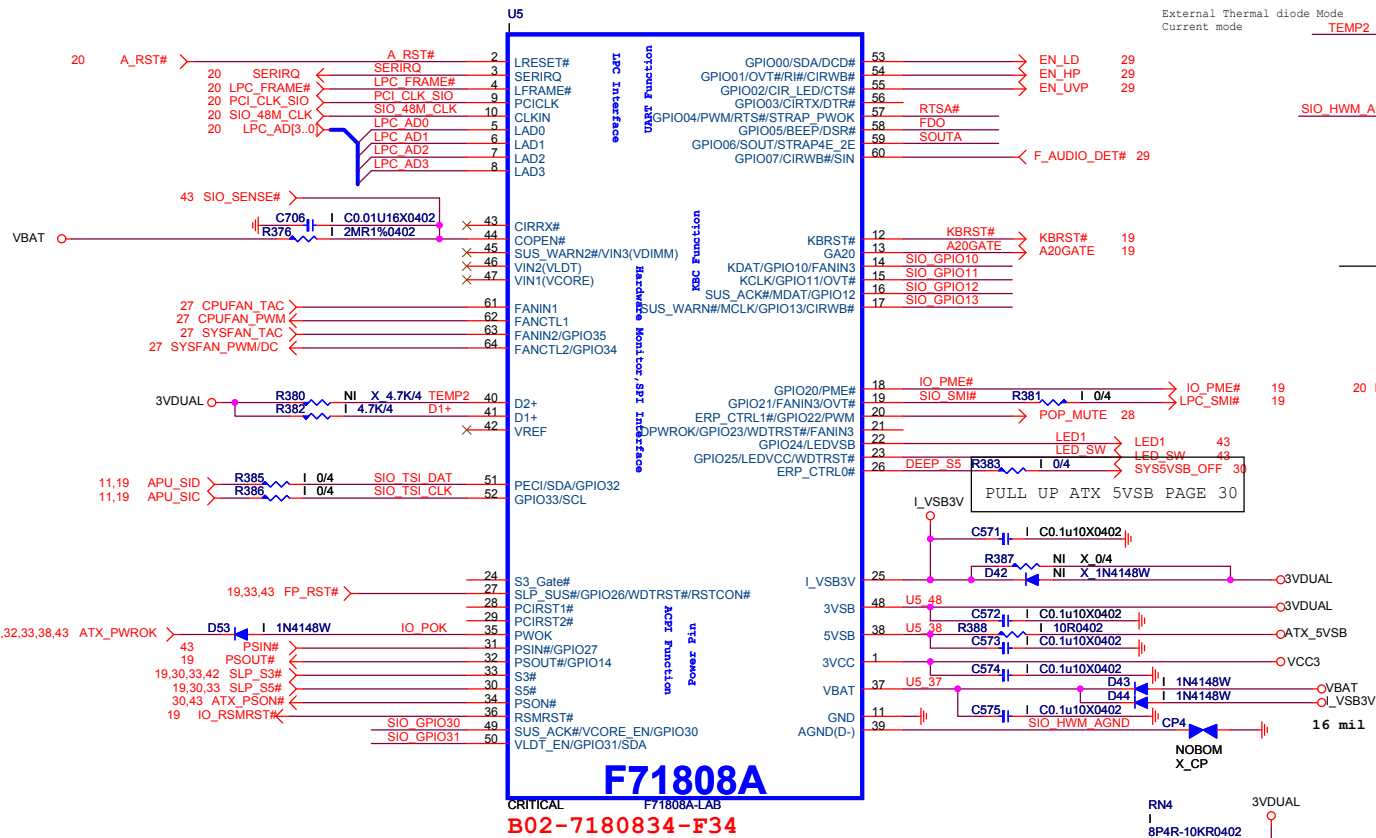


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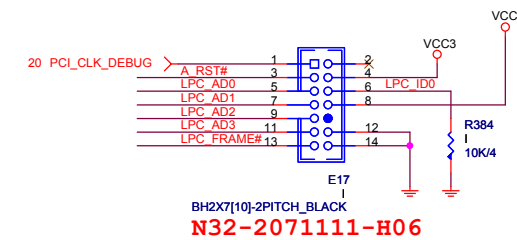
HP SCH P/N: (MSI MS-7778)

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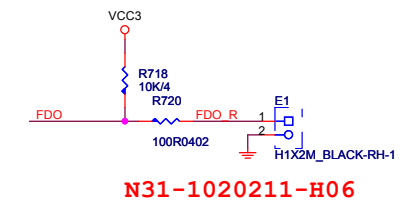
TEMP SENSOR



LPC Debug

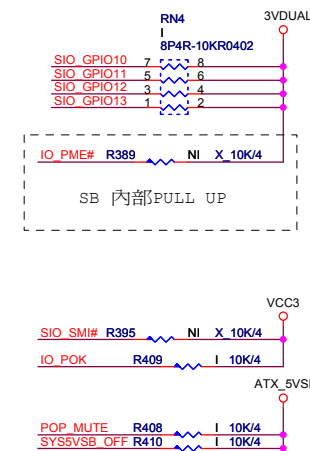
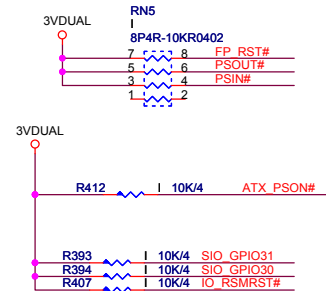
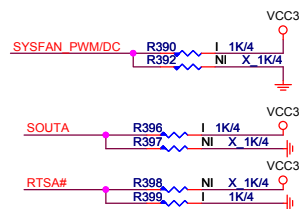


Flash Descriptor Override Header



LPC I/O STRAPPING RESISTOR

POWER-ON TRIP



PIN	Function	NET Name	HI	LO
64	FANCTRL2	FANCTL2	PWM FAN	LINEAR FAN
59	STRAP4E_2E	SOUTA	4E (DEFAULT)	2E
57	STRAP_PWOK	RTSA#	AMD (DEFAULT)	INTEL



MICRO-STAR INT'L CO.,LTD

HP SCH P/N: (MSI MS-7778)

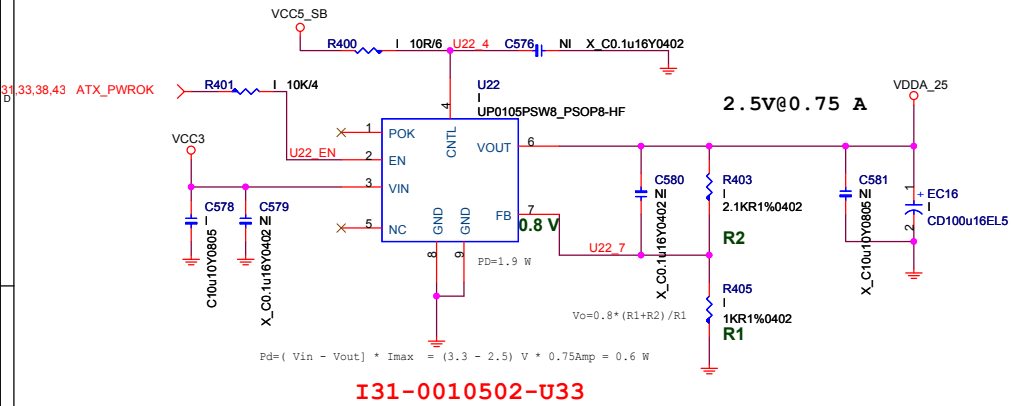
Size Custom	Document Description SUPER I/O F71808A
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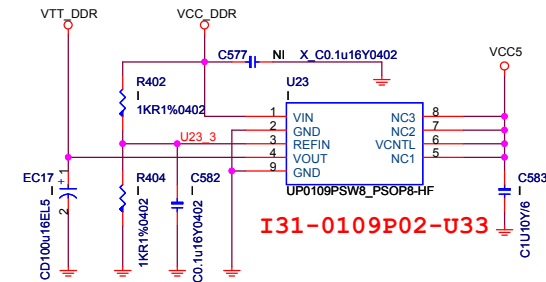
CPU VDDA_25 POWER

Layout:Route 50 mils AND 500 mils LONG
(USE 2x25 mil TRACES TO EXIT BALL FIELD)



VTT_DDR POWER

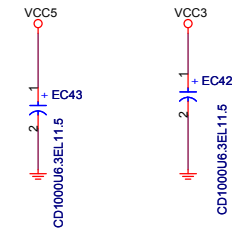
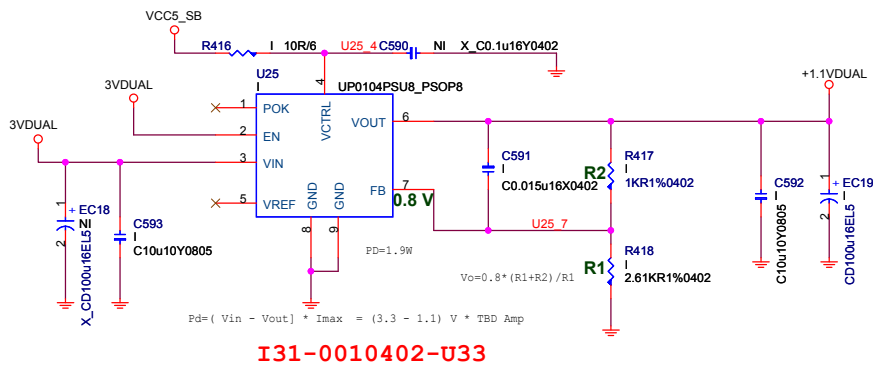
0.75V@2A



1.1VDUAL POWER

1.V@1.3A----D3

S0,S1,S3

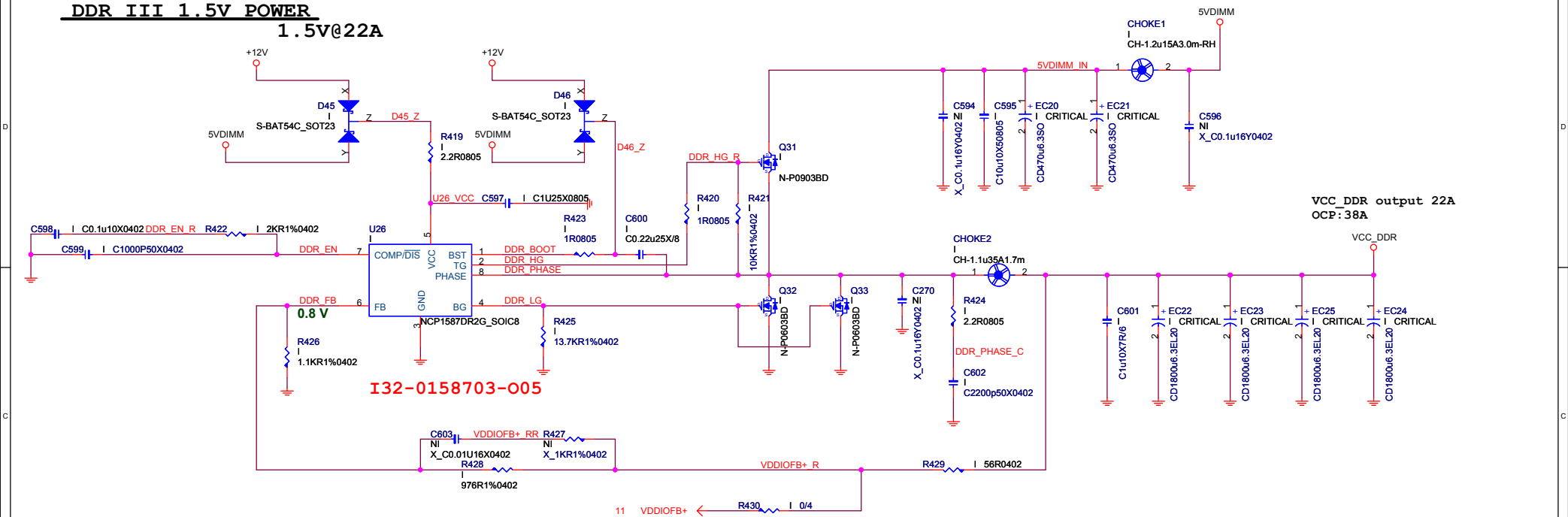


MICRO-STAR INT'L CO.,LTD

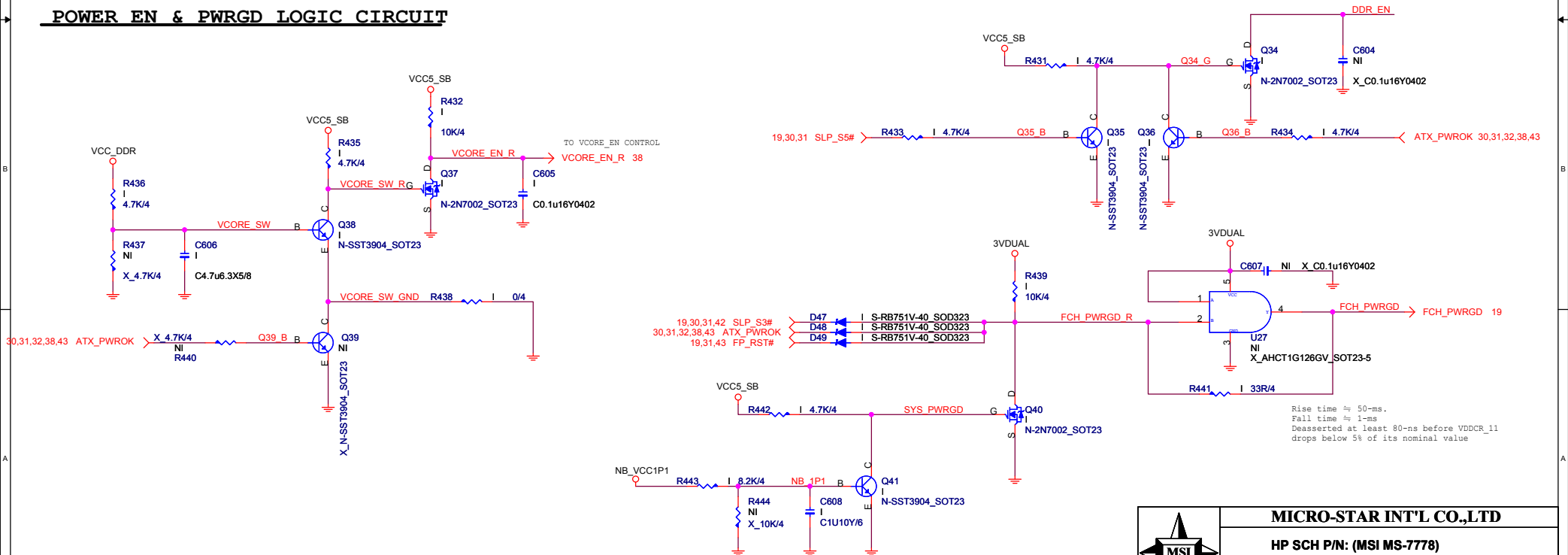
HP SCH P/N: (MSI MS-7778)

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DDR III 1.5V POWER
1.5V@22A



POWER EN & PWRGD LOGIC CIRCUIT



MICRO-STAR INT'L CO.,LTD

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Size	Document Description
100	100
200	200
300	300
400	400
500	500
600	600
700	700
800	800
900	900
1000	1000
1100	1100
1200	1200
1300	1300
1400	1400
1500	1500
1600	1600
1700	1700
1800	1800
1900	1900
2000	2000
2100	2100
2200	2200
2300	2300
2400	2400
2500	2500
2600	2600
2700	2700
2800	2800
2900	2900
3000	3000
3100	3100
3200	3200
3300	3300
3400	3400
3500	3500
3600	3600
3700	3700
3800	3800
3900	3900
4000	4000
4100	4100
4200	4200
4300	4300
4400	4400
4500	4500
4600	4600
4700	4700
4800	4800
4900	4900
5000	5000
5100	5100
5200	5200
5300	5300
5400	5400
5500	5500
5600	5600
5700	5700
5800	5800
5900	5900
6000	6000
6100	6100
6200	6200
6300	6300
6400	6400
6500	6500
6600	6600
6700	6700
6800	6800
6900	6900
7000	7000
7100	7100
7200	7200
7300	7300
7400	7400
7500	7500
7600	7600
7700	7700
7800	7800
7900	7900
8000	8000
8100	8100
8200	8200
8300	8300
8400	8400
8500	8500
8600	8600
8700	8700
8800	8800
8900	8900
9000	9000
9100	9100
9200	9200
9300	9300
9400	9400
9500	9500
9600	9600
9700	9700
9800	9800
9900	9900
10000	10000

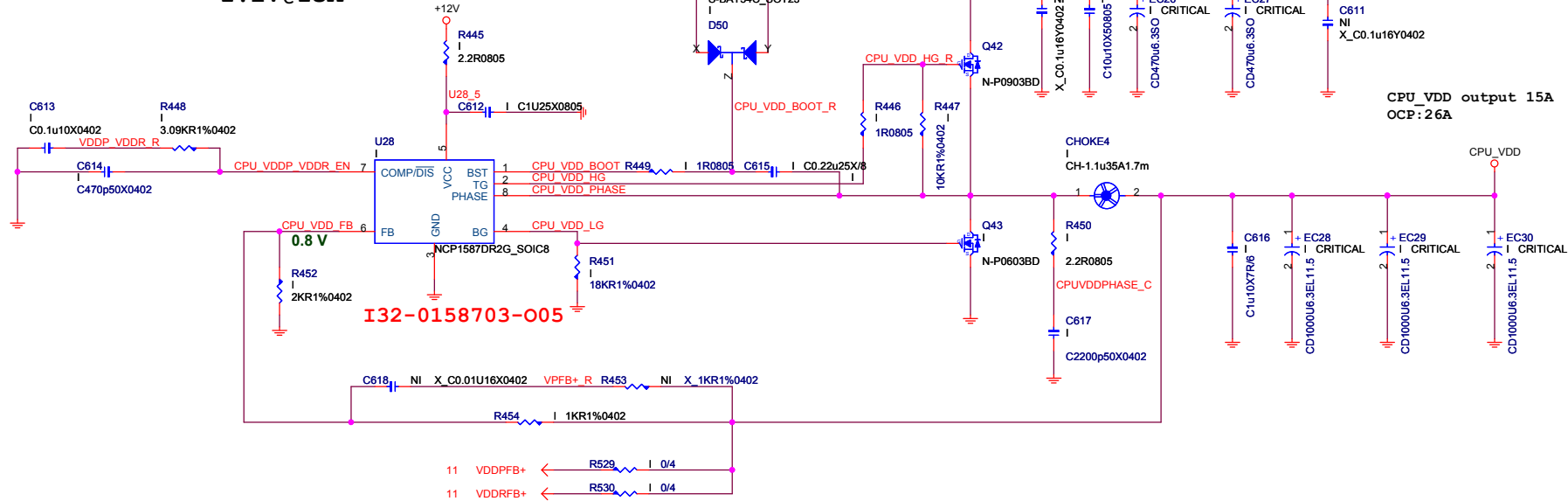
Size	Document Description
Custom	DDR POWER

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0A	

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CPU_VDD POWER

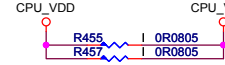
1.2V@15A



VDDP and VDDR support two separate power planes with single regulator

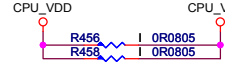
CPU_VDDP POWER

1.2 V@5A



CPU_VDDR POWER

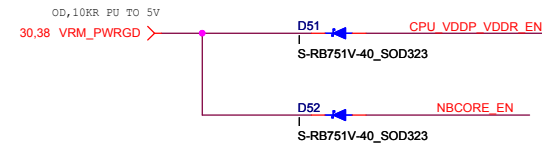
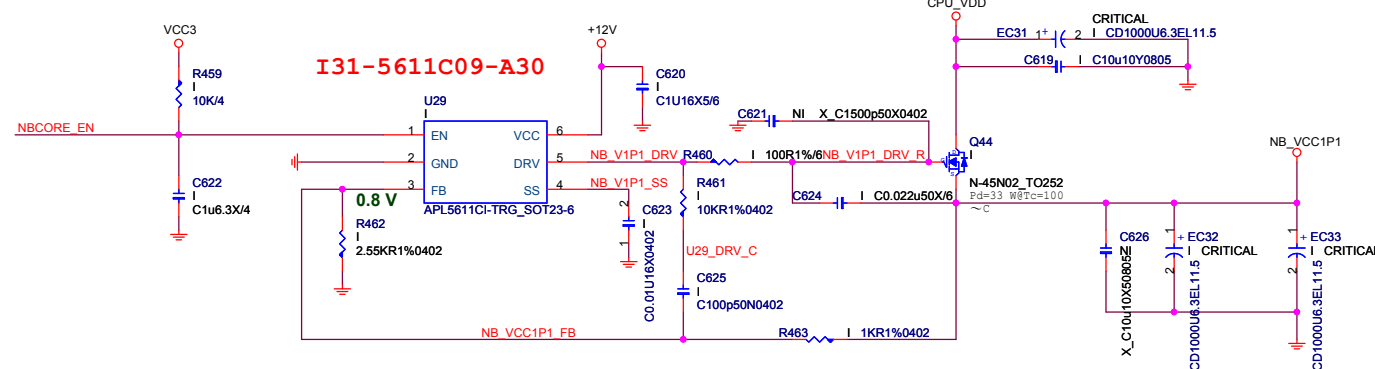
1.2 V@5A



VDDR&VDDP IS COMBINED BY DEFAULT
VDDP_PWMONLY FOR NORMAL OPERATION (VDDR/VDDP COMBINED MODE)
VDDR_PWMIS FOR DEBUG/OC MODE (SEPERATE VDDR/VDDP)

NB_VCC1P1 POWER

1.1V@5A



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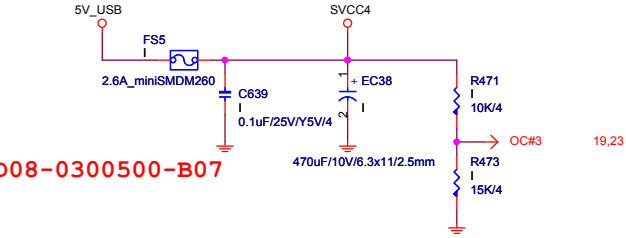
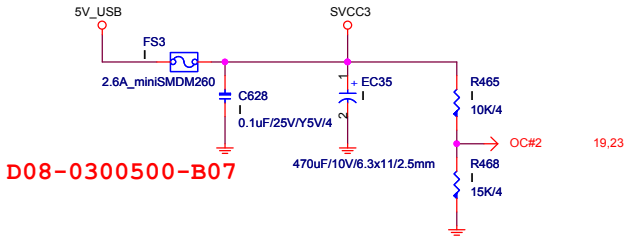
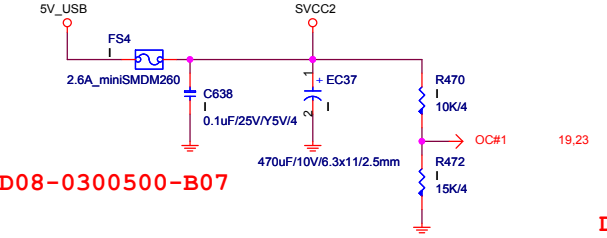
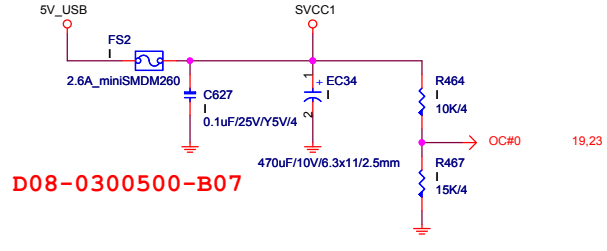
HP SCH P/N: (MSI MS-7778)

Size Custom Document Description FCH CORE

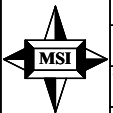
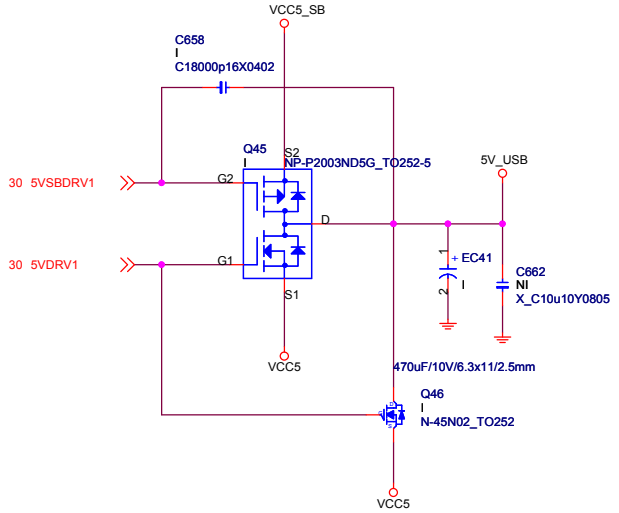
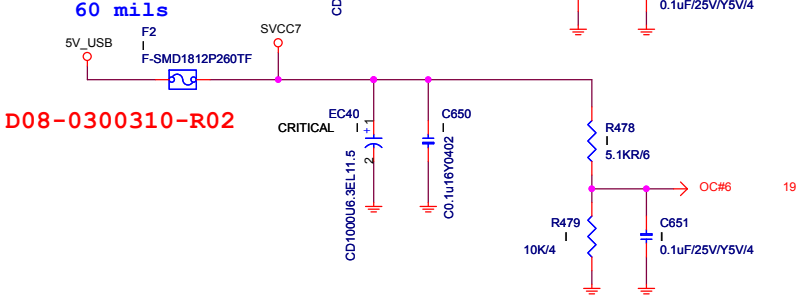
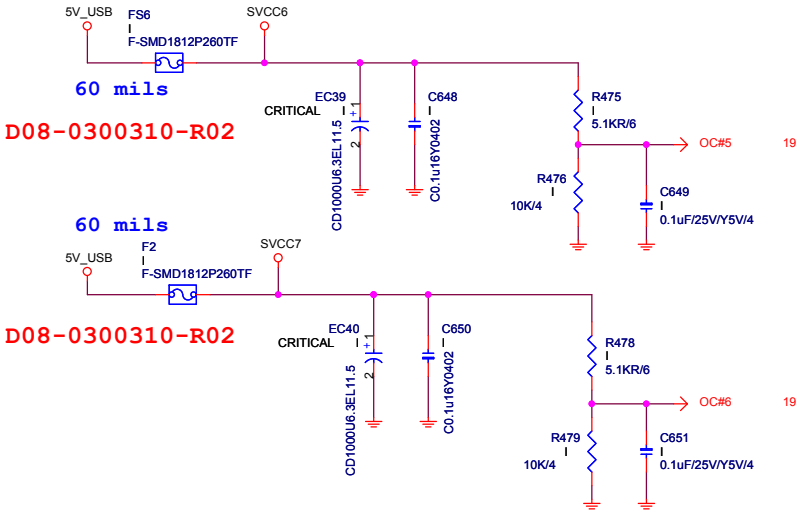
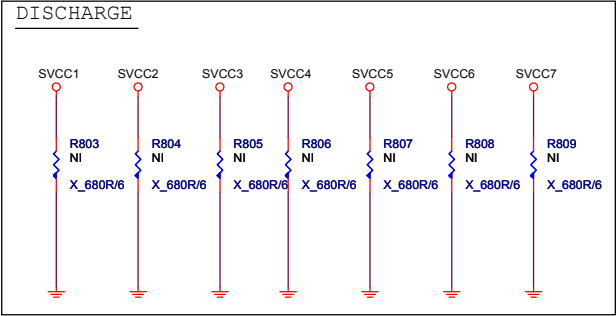
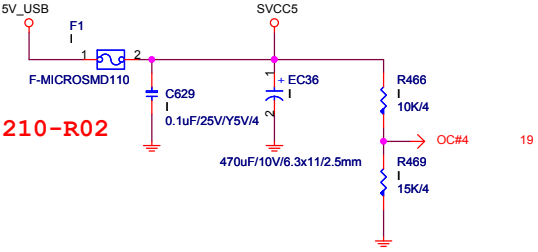
Rev 0A

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USB POWER

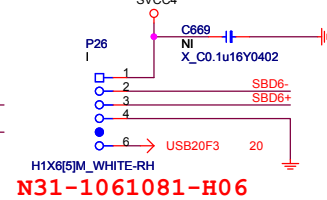
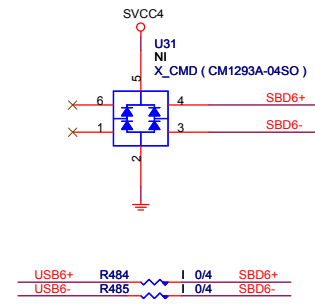
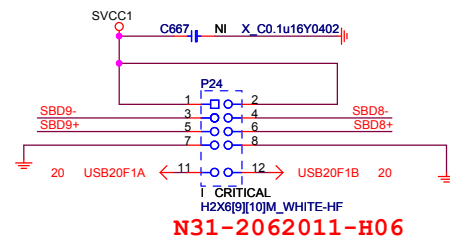
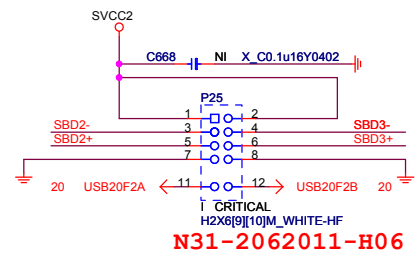
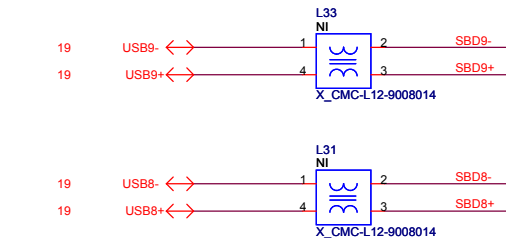
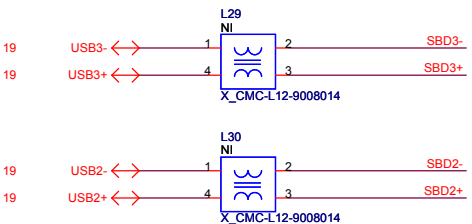
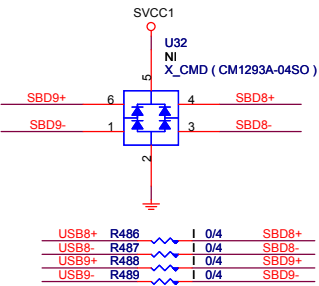
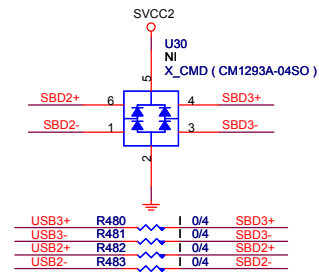


D08-0100210-R02



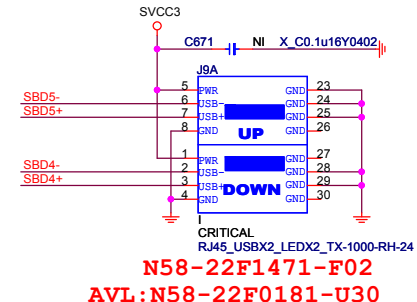
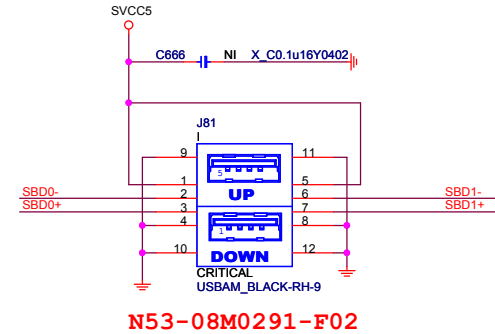
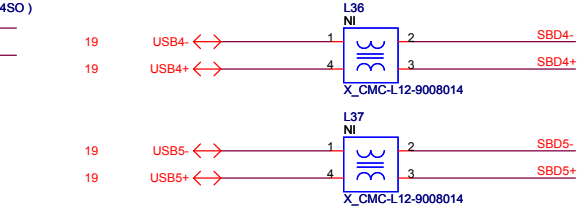
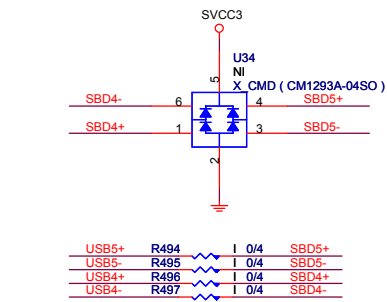
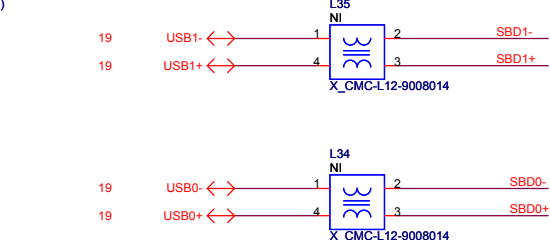
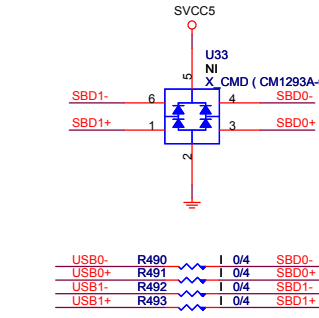
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HP SCH P/N: (MSI MS-7778)		
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USB POWER		
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FRONT USB PIN HEADER



USB 2.0 trace length
FRONT side within 6'';
REAR side within 18''

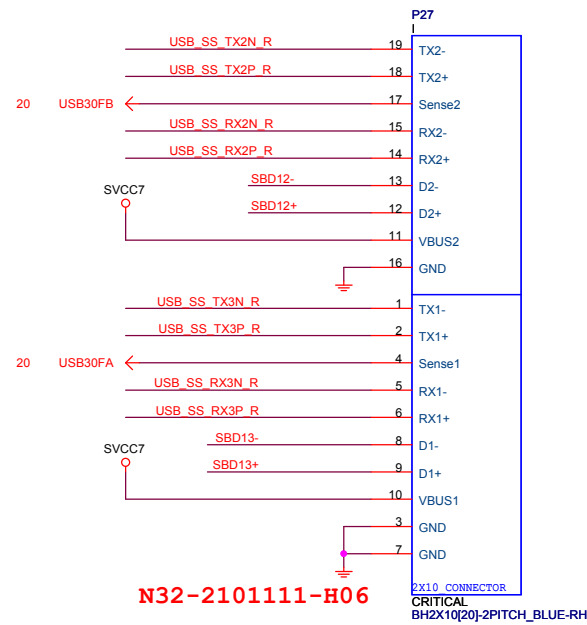
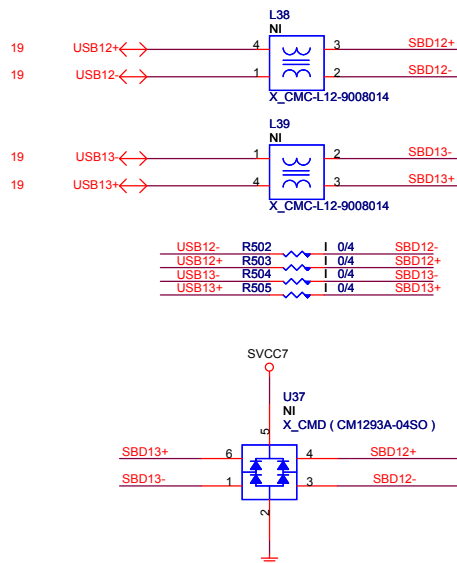
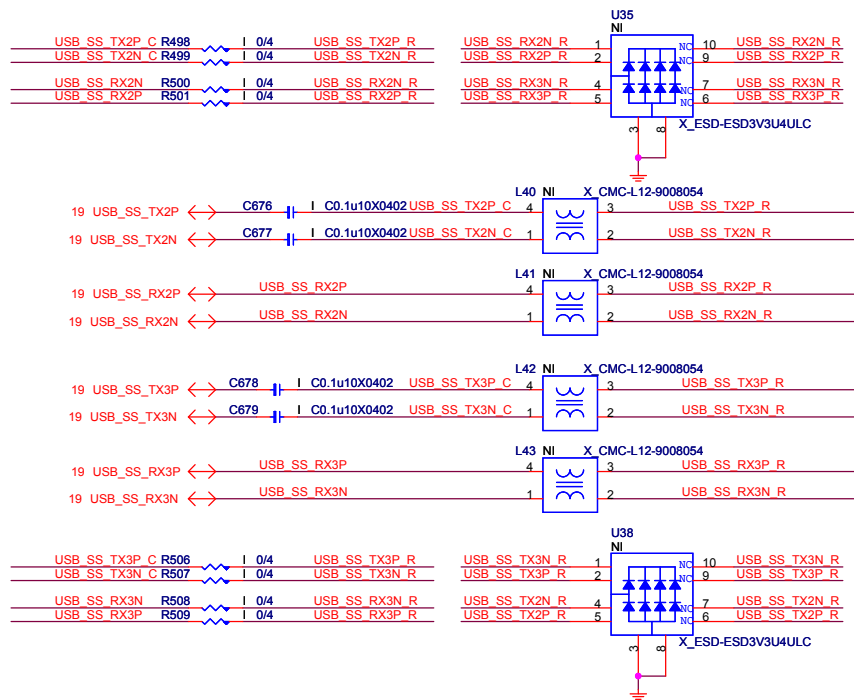
REAR PANEL USB 2.0 CONNECTOR



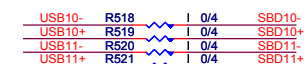
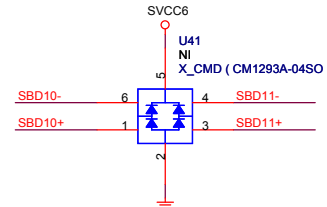
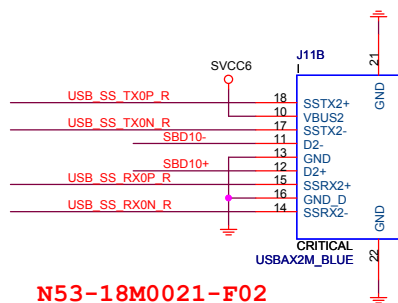
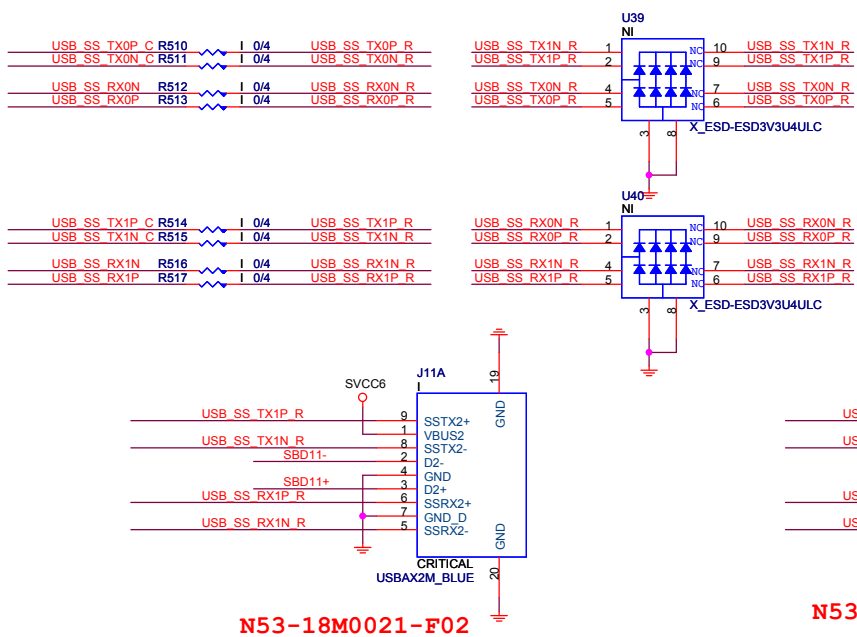


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USB 2.0 CONN		
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USB 3.0 trace length Front pin header within 3.5''



USB 3.0 trace length Rear connector within 8''



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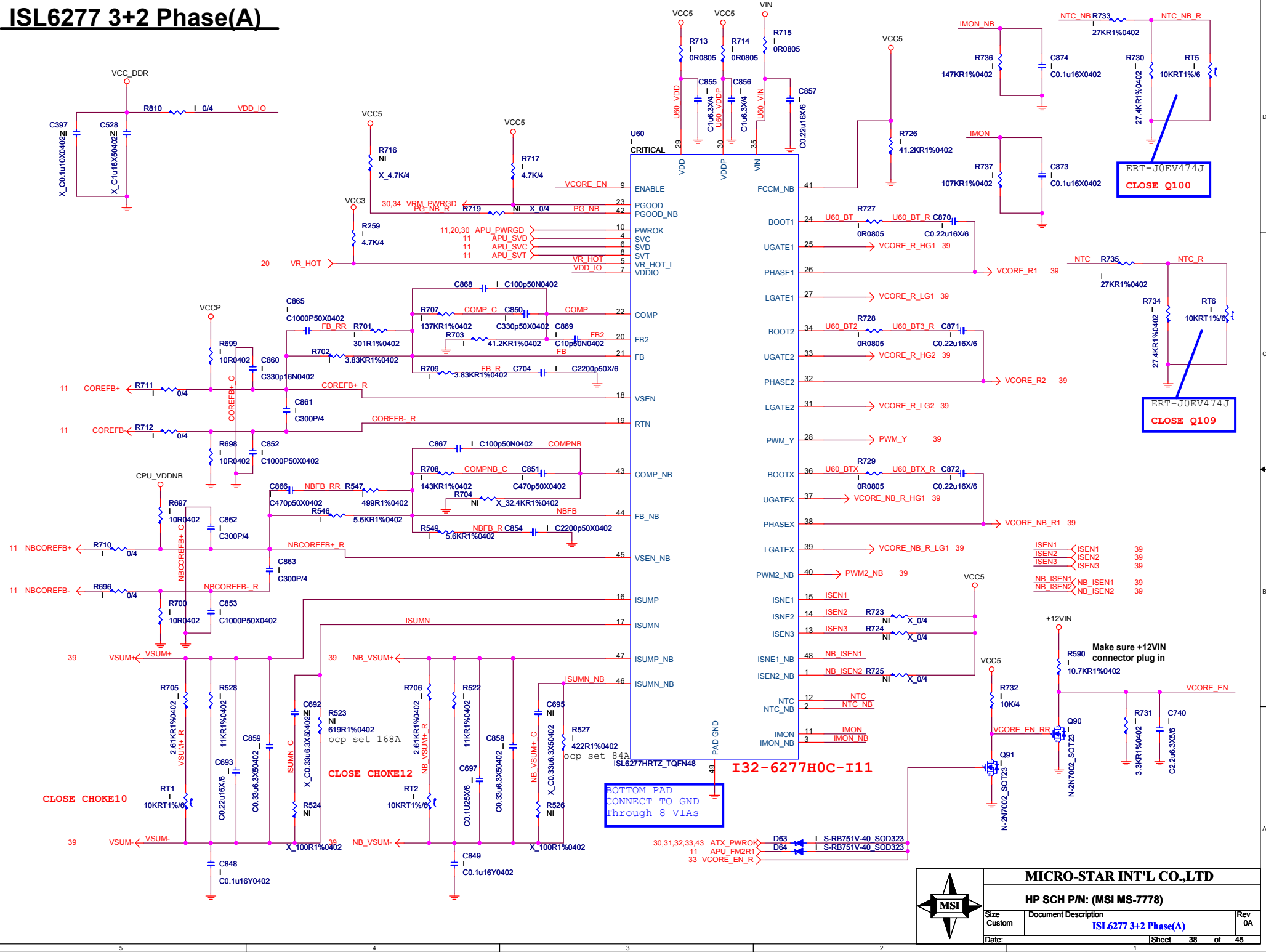
HP SCH P/N: (MSI MS-7778)

Size Custom Document Description
USB 3.0 CONN

Rev 0A

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ISL6277 3+2 Phase(A)



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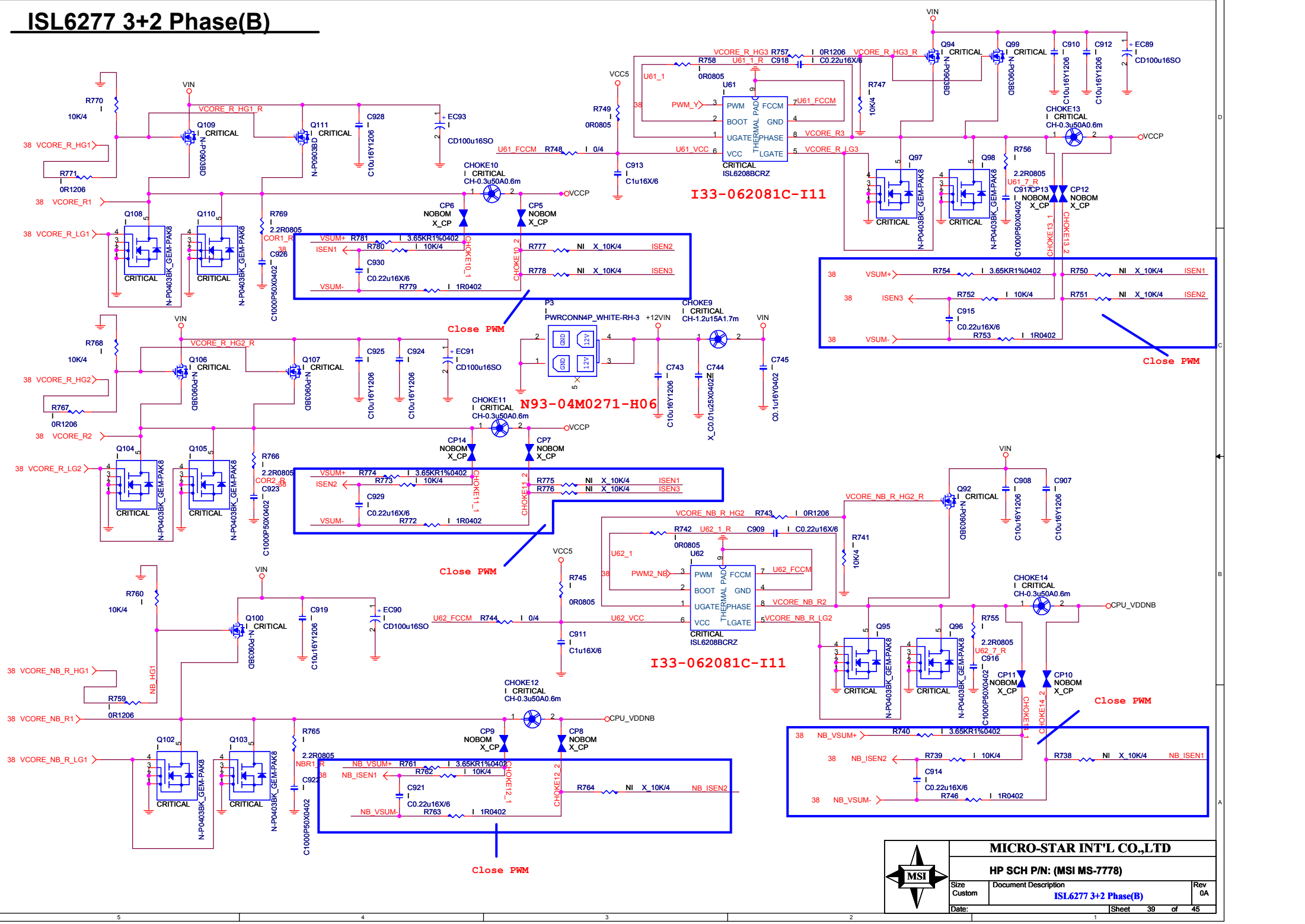
HP SCH P/N: (MSI MS-7778)

Document Description

ISL6277 3+2 Phase(A)

Rev	0A
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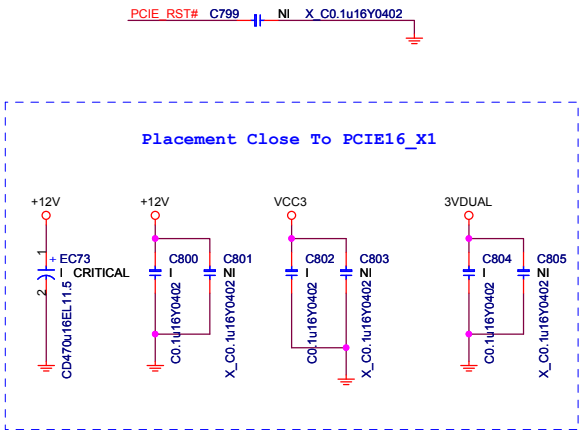
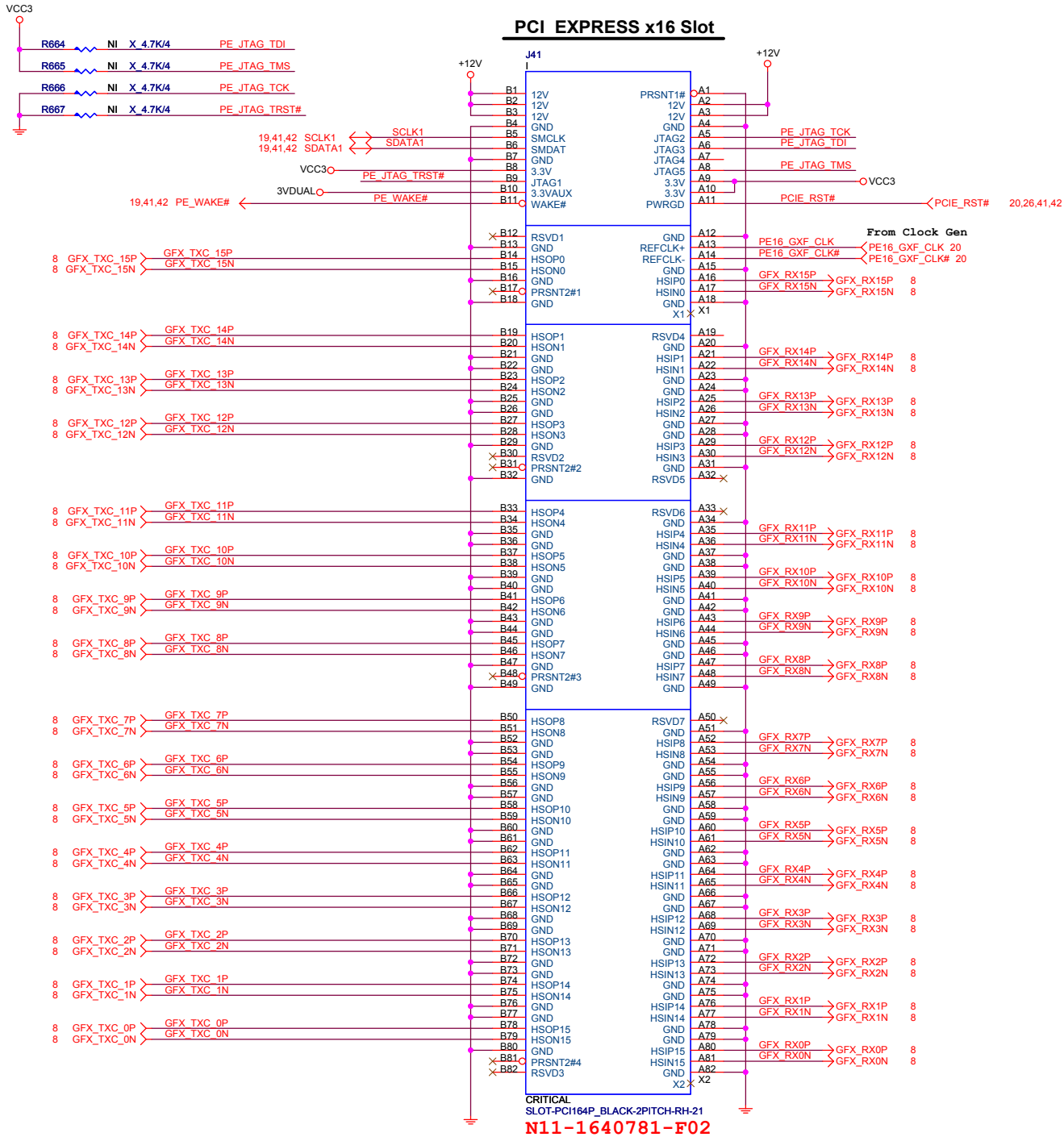
ISL6277 3+2 Phase(B)




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Size Custom	Document Description ISL6277 3+2 Phase(B)	Rev 0A
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PCI Express Slot x16

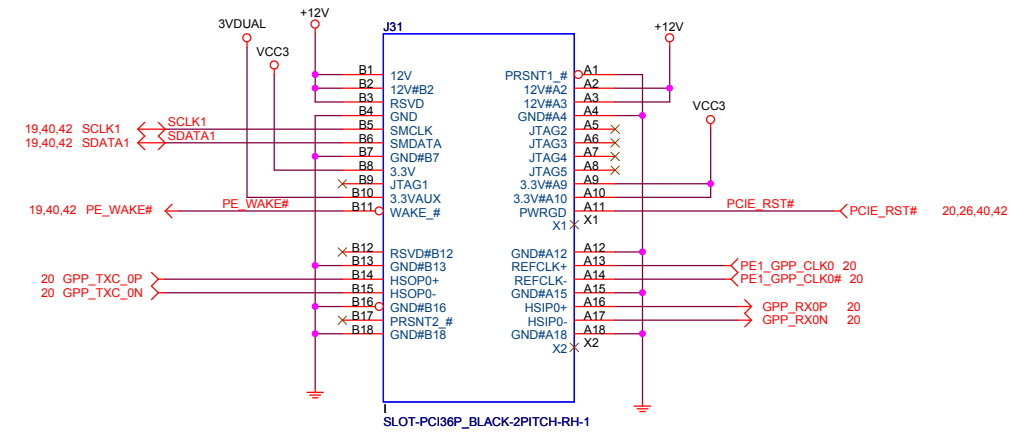
PCI EXPRESS x16 Slot





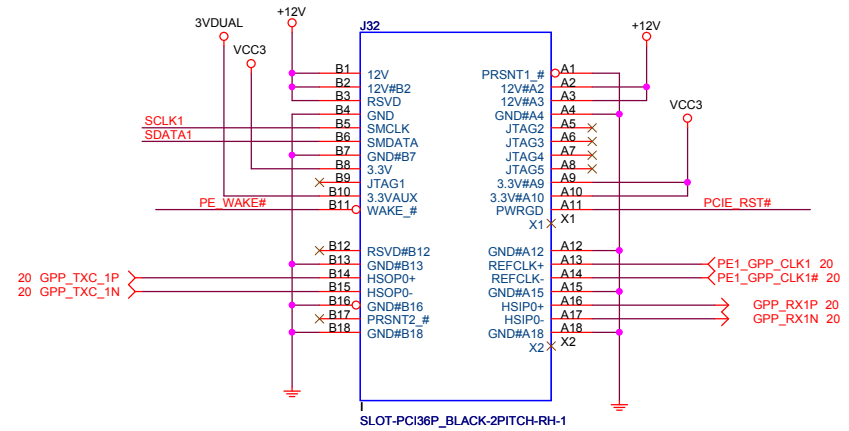
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PCIE X16 SLOT		
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PCI EXPRESS X1 Slot-1



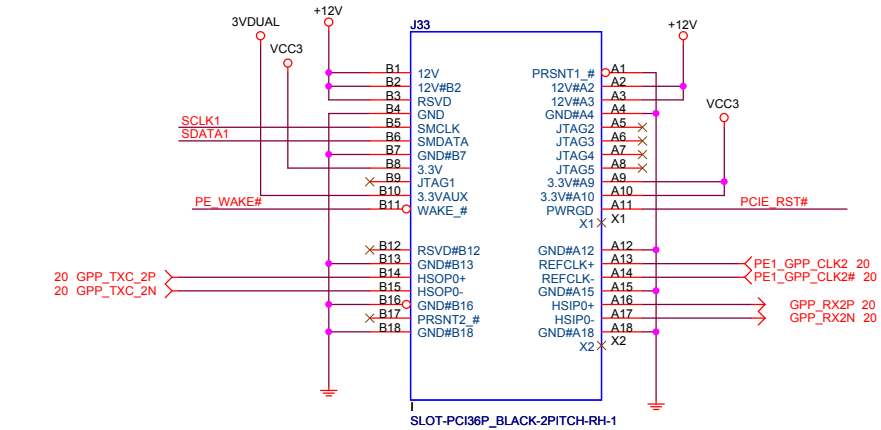
N11-0360251-F02

PCI EXPRESS X1 Slot-2

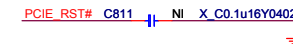
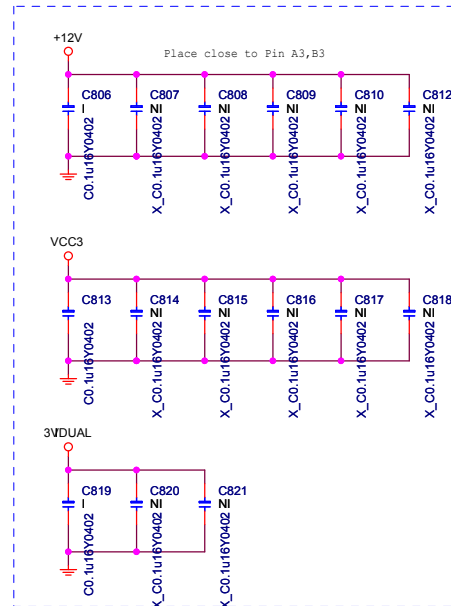


N11-0360251-F02

PCI EXPRESS X1 Slot-3



N11-0360251-F02



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Size
Custom

Document Description

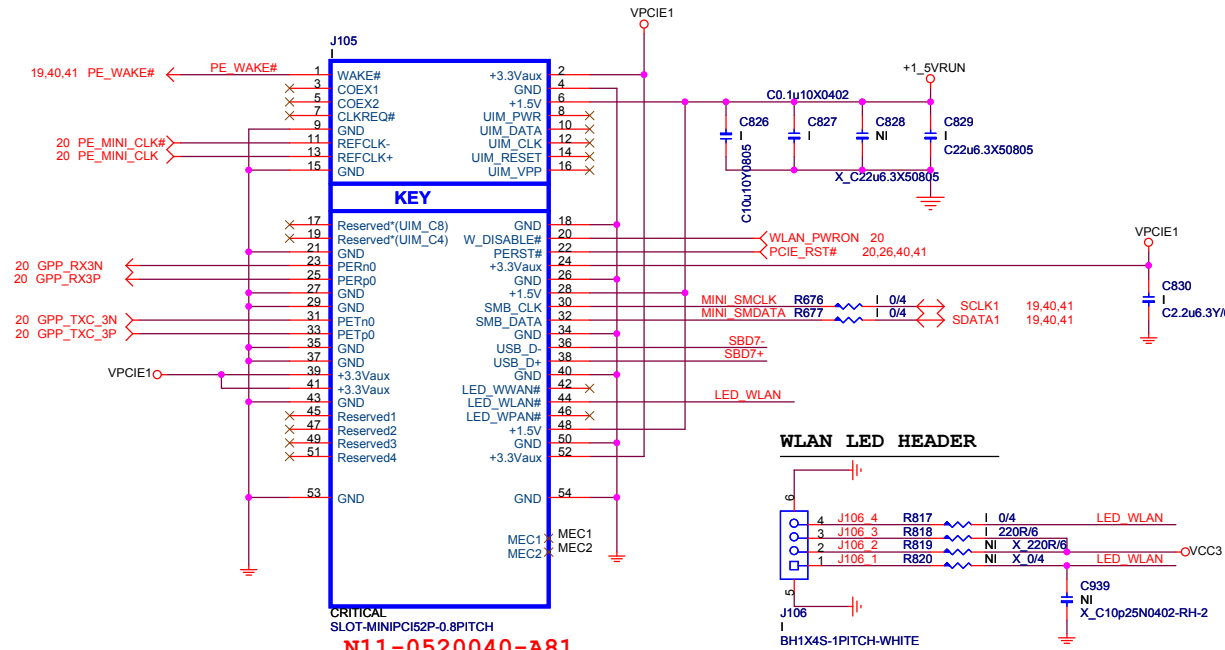
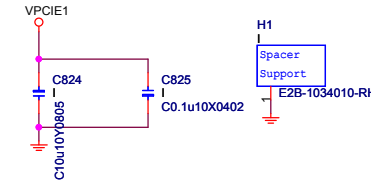
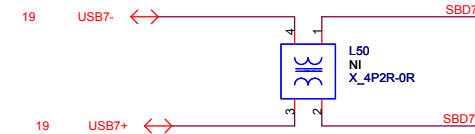
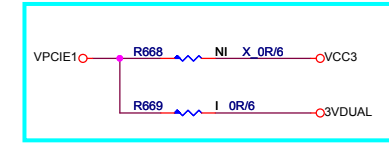
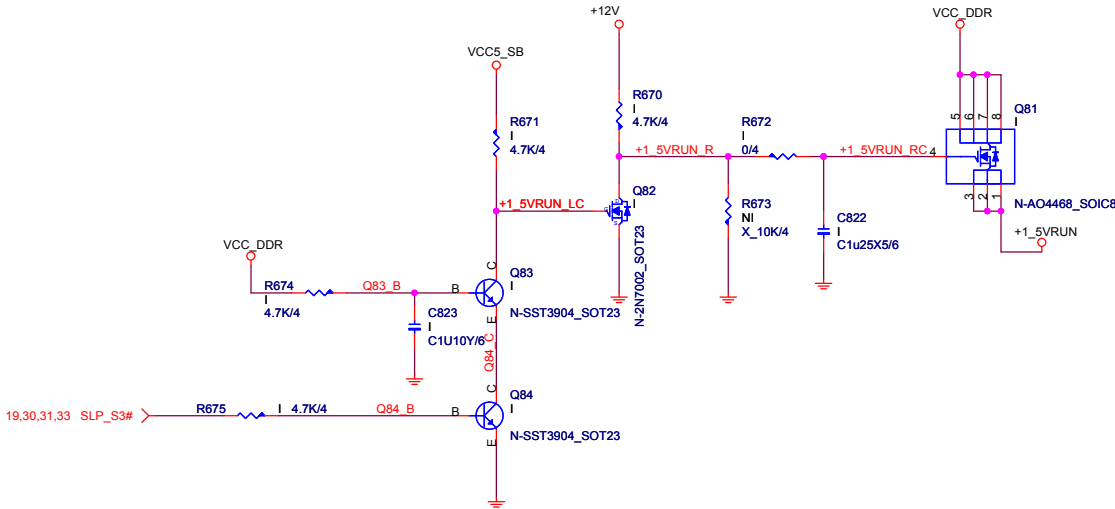
PCI EXPRESS X1 SLOTS

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Wireless LAN(Short Card)



N11-0520040-A81

N32-1040440-H06



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Intel Front Panel

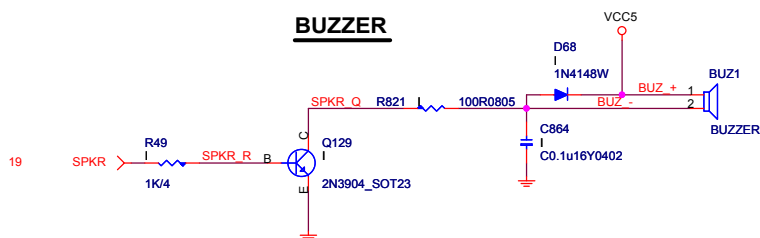


P125--HOOD-SENSE-HEADER-PIN-DESCRIPTION:

Diagram illustrating the HOOD_SENSE# signal line connection:

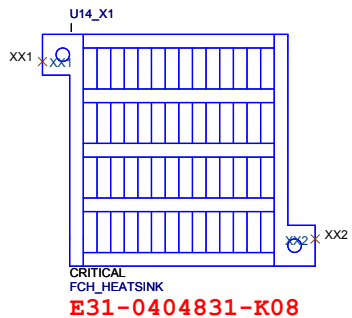
- The signal line is pulled up to VCC3 by an 8.2K/4 resistor (R683).
- The signal line is connected to pin 1 of the BHTX3B-FR_WHITE-HF connector.
- Pin 2 is connected to the SIO_SENSE# signal.
- Pin 3 is connected to ground.

ATX CONNECTOR

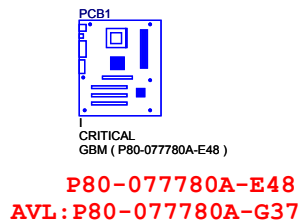


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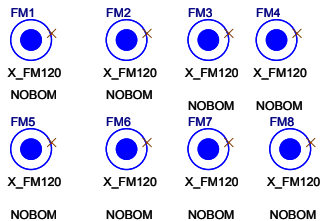
HEAT SINK



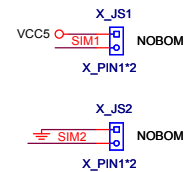
MANUAL PART



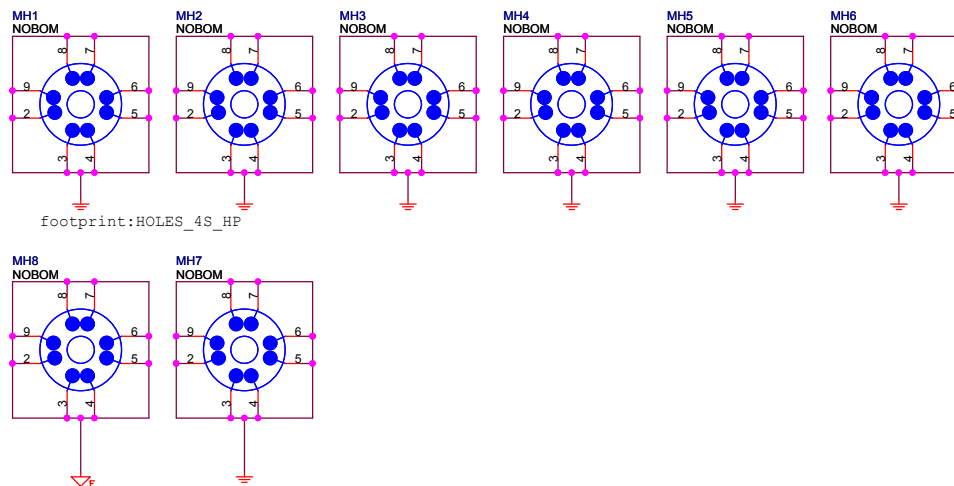
Optics Orientation Holes



Simulation



Mounting Holes



1

C

3

A



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